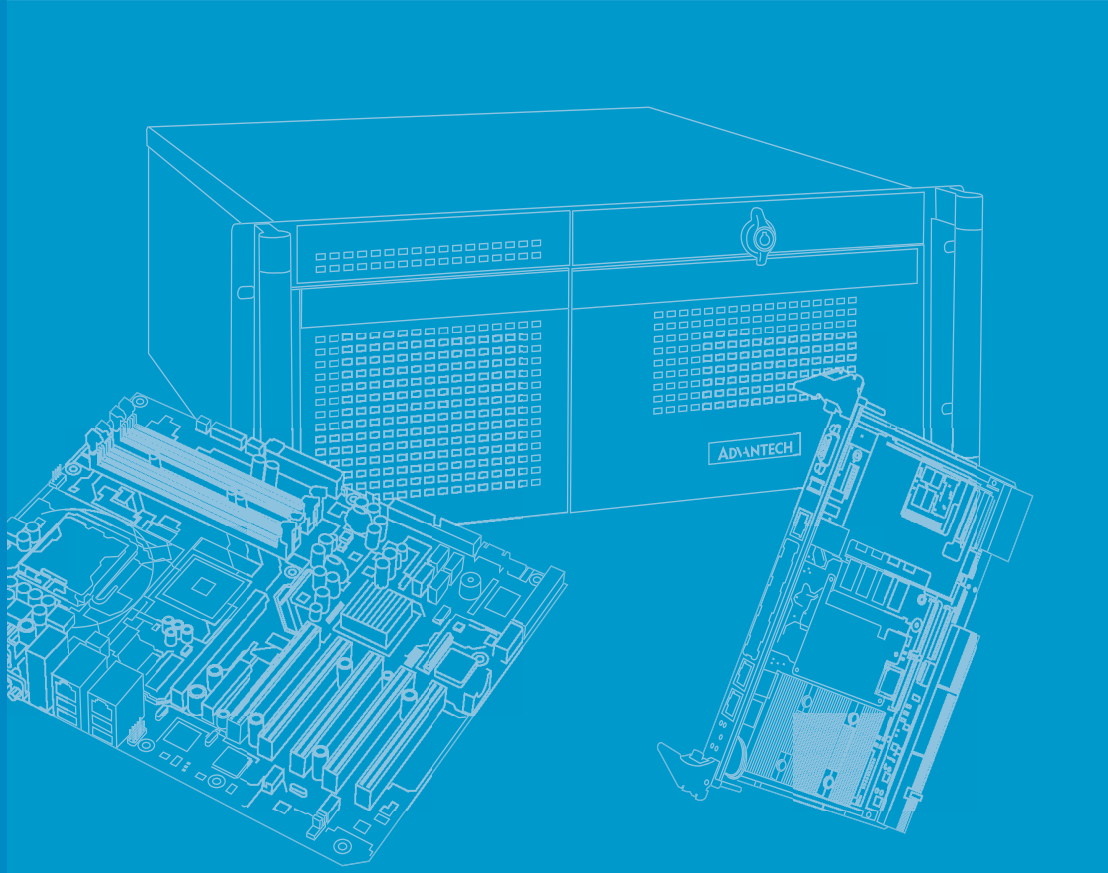

User Manual

ITA-5831 Series

Intel® the 6rd Generation Core™ i Processor Fanless System for Railway Applications

ADVANTECH

Enabling an Intelligent Planet

Copyright

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All other product names or trademarks are properties of their respective owners.

Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

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Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

A Message to the Customer

Advantech Customer Services

Each and every Advantech product is built to the most exacting specifications to ensure reliable performance in the harsh and demanding conditions typical of industrial environments. Whether your new Advantech equipment is destined for the laboratory or the factory floor, you can be assured that your product will provide the reliability and ease of operation for which the name Advantech has come to be known. Your satisfaction is our primary concern. Here is a guide to Advantech's cus- tomer services.

To ensure you get the full benefit of our services, please follow the instructions below carefully.

Technical Support

We want you to get the best performance possible from your products. If you run into technical difficulties, we are here to help. For the most frequently asked questions, you can easily find answers in your product documentation. These answers are normally a lot more detailed than the ones we can give over the phone.

Please consult this manual first. If you still cannot find the answer, gather all the information or questions that apply to your problem, and with the p can be assured that your product will provide the reliability and ease of operation for floor, you can be assured that your product will provide the reliability and ease of o oy product close at hand, call your dealer. Our dealers are well trained and ready to give you the support you need to get the most from your Advantech products. In fact, most problems reported are minor and can be easily solved over the phone.

In addition, free technical support is available from Advantech engineers every business day. We are always ready to give advice about application requirements or specific information on the installation and operation of any of our products.

Initial Inspection

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- 1 x ITA-5831 series industrial computer
- 1 x ITA-5831 accessory box
- 1 x Warranty card

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We have carefully inspected the ITA-5831 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the ITA-5831, check it for signs of ship- ping damage. (For examples: box damage, scratches, dents, etc.) If it is damaged or it fails to meet the specifications, notify our service department or your local sales representative immediately. Also, please notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment does not work well, or you cannot get it to work according to the user's manual.
    - The equipment has been dropped and damaged.
    - The equipment has obvious signs of breakage.

15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -40° C (-104° F) OR ABOVE 55° C (131° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

Battery Information

Batteries, battery packs and accumulators should not be disposed of as unsorted household waste. Please use the public collection system to return, recycle, or treat them in compliance with the local regulations.

Warnings, Cautions and Notes

Warning! *Warnings indicate conditions, which if not observed, can cause personal injury!*

Caution! *Cautions are included to help you avoid damaging hardware or losing data. e.g.There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*

Note! *Notes provide optional additional information.*

Contents

Chapter 1

Overview

Sections include:

- Introduction
- Specifications
- Power Information
- Environment Specifications
- Dimension Diagram

1.1 Introduction

The ITA-5831 is a fanless, compact embedded industrial computer chassis with the 6th Gen Core™ i processor and wide voltage input range, which is specially designed for intelligent transportation and road surveillance. This powerful computing platform can withstand operation 24 hours a day, 7 days a week.

1.2 Specifications

- **Processer and Chipset:** Intel® Core™ i7/i5/Celeron processor + QM170 chipset
- **BIOS: AMI SPI 16M byte Flash**
- **Memory:** On-board 8 GB DDR4 2133 MHz
- **Display:** Intel® HD Graphics 530 (Core i)
  - VGA: 1920x1200 @ 60 Hz
  - DVI: 1920x1200 @ 60 Hz
- **DP extension:**
  - HDMI: 4096x2160 @ 24 Hz, 24 bpp
  - DVI: 1920x1200 @ 60 Hz
  - VGA: 1920x1200 @ 60 Hz
- **EDP extension:** LVDS
- **Storage:** Supports 2 x 2.5" SSD (Default setting, 1 x ITA-EM-ST51-00A1E)
  - Max to 3 x 2.5" SSD
  - 1 x Full-size mSATA (on Mainboard)
- **Expansion:** 3 x Full-size Mini PCIe Socket
- **Ethernet:** 3 x 10/100/1000Mbps with M12 X-coded (Female) Controller: Intel I210-IT
- **USB:** 2 x USB3.0 with Type A, 1 x USB2.0 with M12 A-coded (F) 4-pin
- **DVI:** 1 x DVI-I
- **Series I/O:** 2 x RS-232/422/485 with 2KV Isolation; support auto-flow control, DB9 type
- **Digital I/O:** 1 x 4-bit DI/4-bit DO with 2KV Isolation
- **Audio:** 1 x Speaker-out with 2 x 4W Amp., 1 x Mic-in
- **Optional I/O modules:**
  - 1 x ITA-EM-SR61(ITAM-SR51): 4 x RS232/422/485 with 2KV Isolation
- **Dimension (W x H x D):**
  220 x 88 x 198.8 mm
  256 x 92 x 198.8 mm with mounting kits
- **Net weight:** 4.5 Kg

1.3 Power Information

ITA-5831 power design complies with EN 50155 S2/C1.

Table 1.1: Power input				
DC-IN Voltage	24V	48V	72V	110V
Voltage Range (0.7~1.25)	16.8 ~ 30V	33.6 ~ 60V	50.4 ~ 90V	77 ~ 137.5V
Transient (0.6~1.4/0.1s)	14.4 ~ 33.6V	28.8 ~ 67.2V	43.2 ~ 100.8V	66 ~ 154V
Power connector	1 x M12 S-coded (M) 4-pin			

1.4 Environmental Specifications

Table 1.2: Environmental Specifications	
Operating Temperature	EN50155 Tx level: -40 ~ 70°C (with industrial storage)
Safety Certificate Temperature	-10~50°C (with industry level accessory)
Storage Temperature	-40 ~ 85°C
Humidity	95% @ 40º C, non-condensing
Vibration	1 Grms @ 5 ~ 500 Hz, random, 1 hr/axis (SSD/mSATA)
Bump	10G, IEC60068-2-27:1987, half-sine wave, 16 ms duration
Safety	UL, CCC, BSMI, CE, FCC

The shock and vibration tests were conducted according to the Category 1.
Body mounted Class B of the EN 61373 with the acceptable results.

1.5 Dimension Diagram

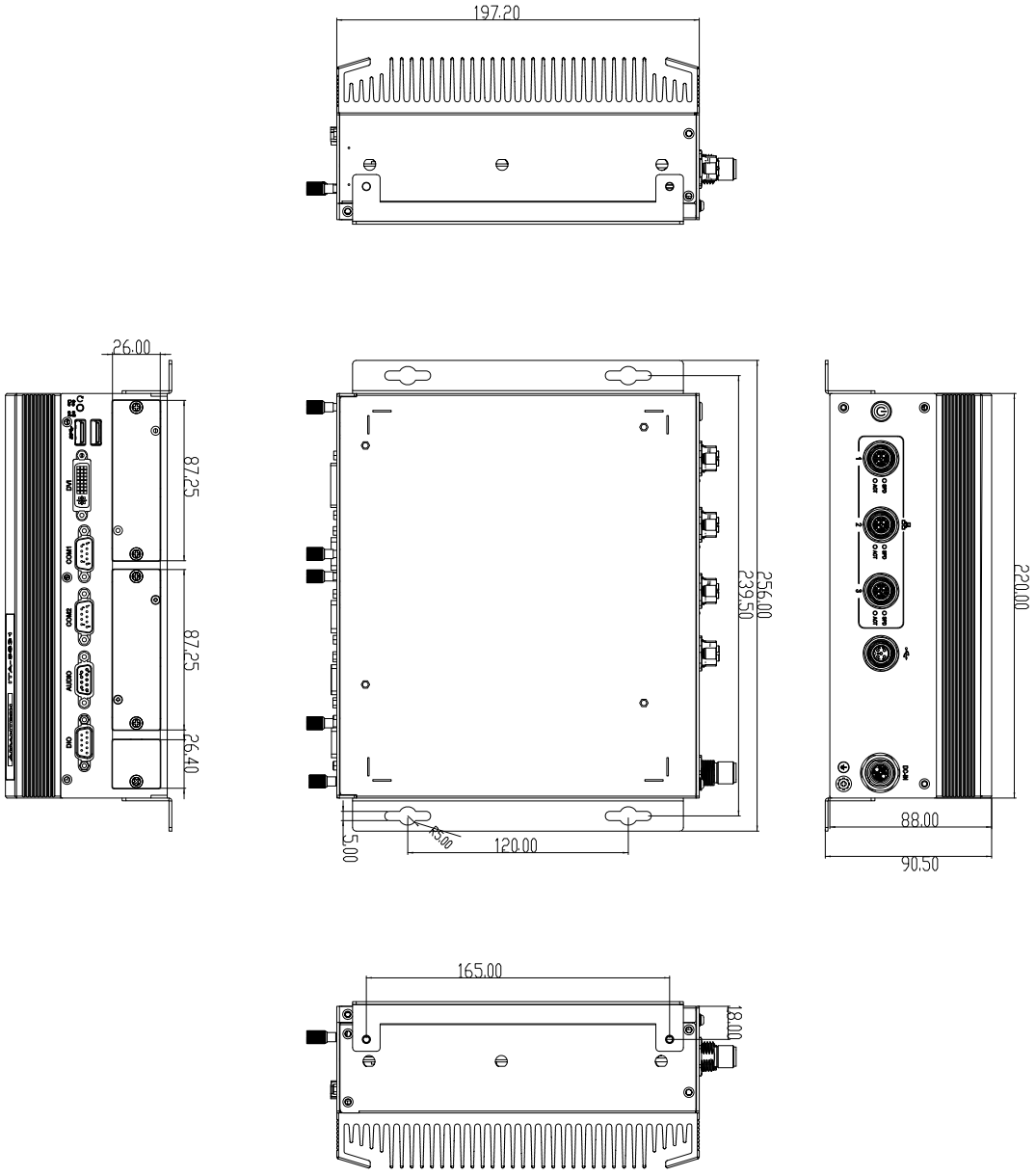


Figure 1.1 Dimension Diagram of ITA-5831

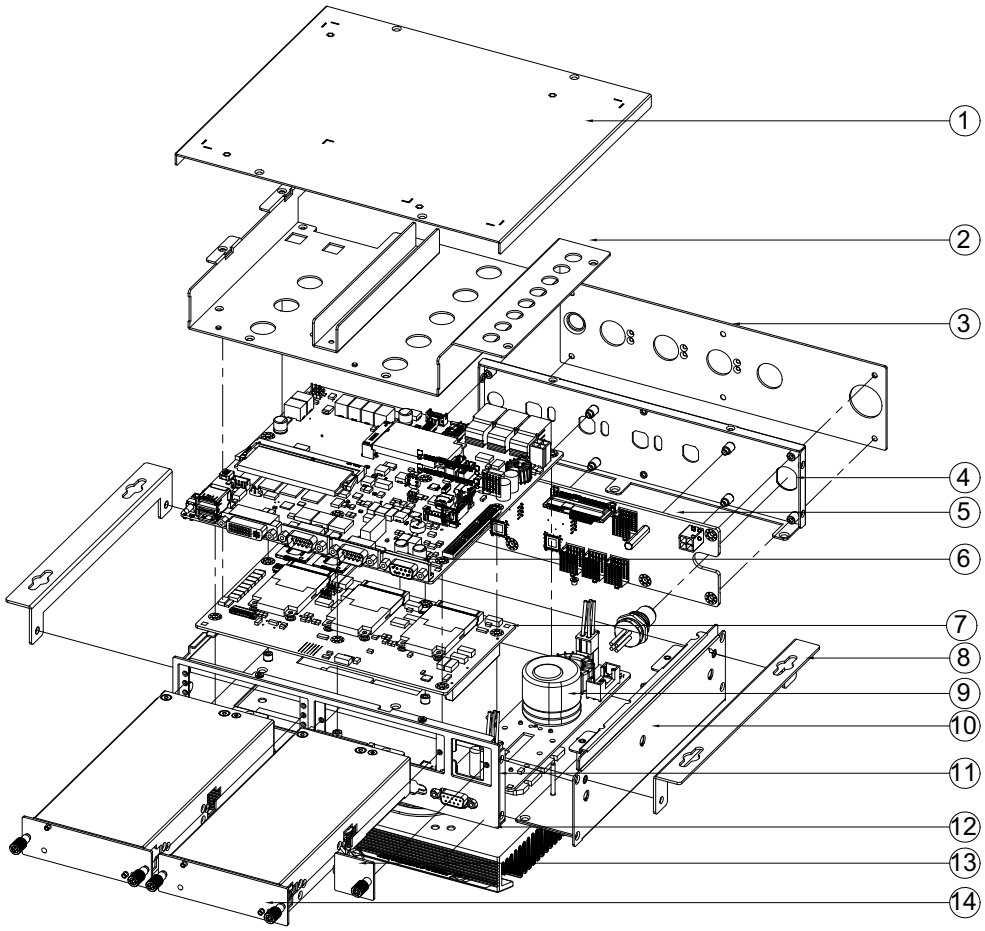


Figure 1.2 Exploded Diagram of ITA-5831

Table 1.3: Parts list			
1	Top cover	8	Mounting kits
2	Carrier board for easy-swap module	9	Power module
3	Real I/O panel	10	Power module bracket
4	Front panel (Internal)	11	Front panel (Internal)
5	Backplane	12	Front panel
6	Main board	13	Heatsink
7	Carrier board	14	Easy-swap module (Optional)

Chapter 2

H/W Installation

Sections include:

- Introduction
- Jumpers and Connectors
- I/O Connectors

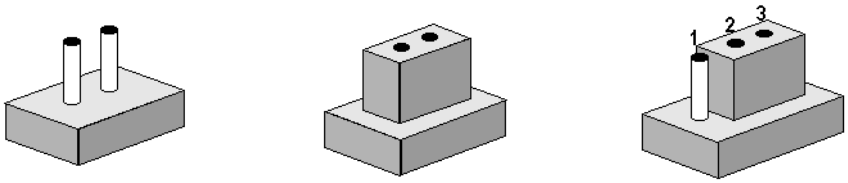
2.1 Introduction

The following sections show the internal jumpers setting and the external connectors pin assignment for application integration.

2.2 Jumpers and Connectors

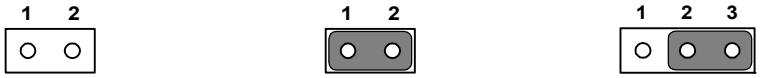
2.2.1 Jumper Description

You may configure the ITA-5831 to match the needs of your application by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To close a jumper, you remove the clip. Sometime a jumper will have three pins, labelled 1, 2 and 3. In this case you would connect either pins 1 and 2, or 2 and 3.



Open Closed 2-3 Closed

The jumpers setting are schematically depicted in this manual as follows.



Open Closed 2-3 Closed

A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes. Generally, you simply need a standard cable to make most connections.

2.2.2 Jumper and Connector Location

The main board has a number of connectors and jumpers that allow you to configure your system to suit your application. The table below lists the function of each of the connectors and jumpers. The locations of jumpers and connector on board are shown in Figure 2.1.

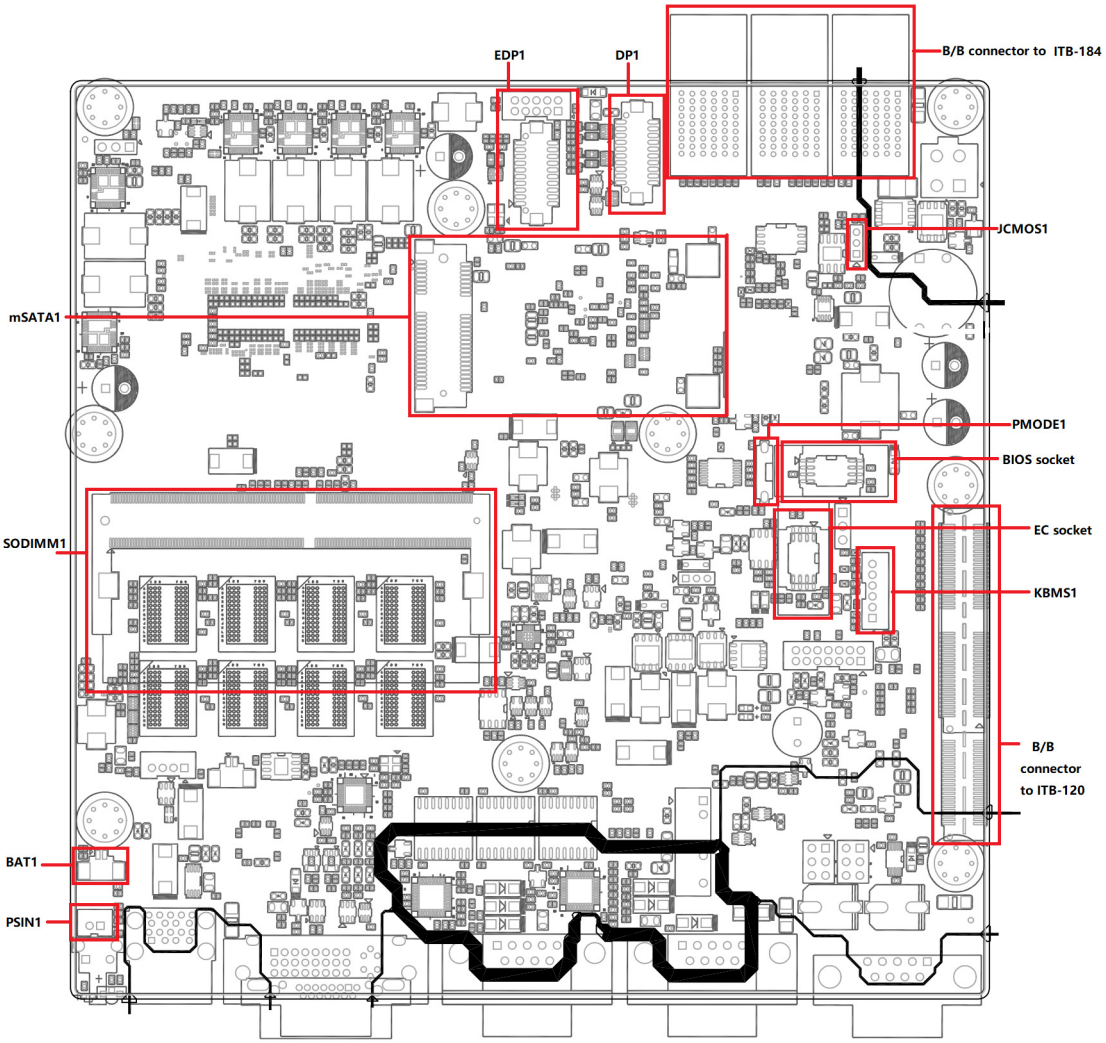


Figure 2.1 Jumpers and Connector Location on Main Board

Table 2.1: Jumpers and switches

Name	Function
PSIN1	Power button pin header
BAT1	RTC battery pin header
JCOMS1	Clear CMOS setting
PMODE1	ATX, AT mode switch

Table 2.2: BAT1(RTC battery pin header)	
Pin	**Setting**
1	Power(3.3V)
2	GND
*Default setting	

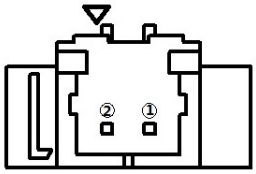


Table 2.3: JCMOS1(Clear CMOS setting)	
Pin	**Setting**
1-2	Default*
2-3	Clear CMOS
*Default setting	

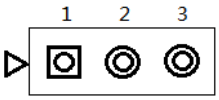
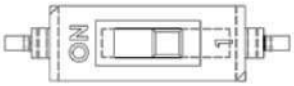


Table 2.4: PMODE1(AT,ATX witch)	
Pin	**Setting**
On	AT
Off	ATX *
*Default setting	



2.3 I/O Connectors

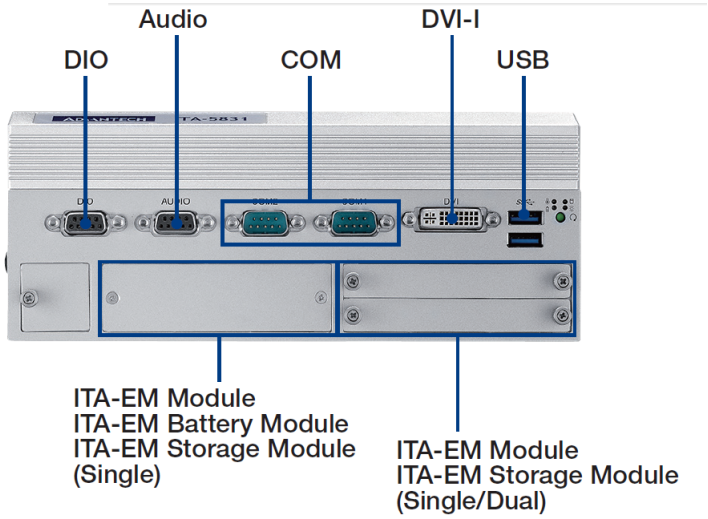


Figure 2.2 ITA-5831 Front View

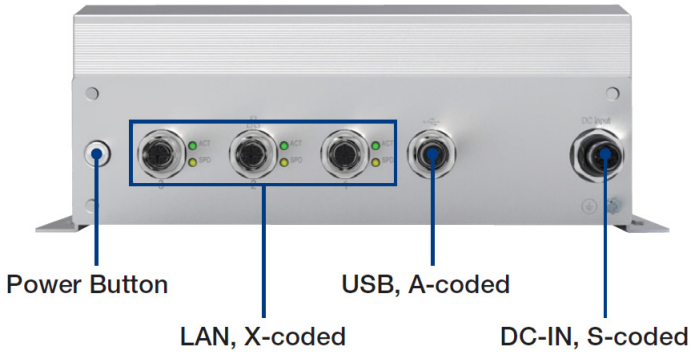


Figure 2.3 ITA-5831 Real View

2.3.1 COM connector

ITA-5831 provides two RS-232/422/485 DB9 connectors. The default setting is RS-232.

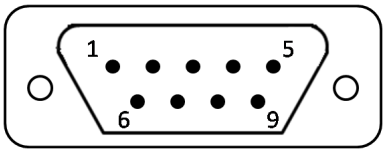


Table 2.5: COM Connector Pin Definition

	RS-232	RS-422	RS-485
Pin	**Signal Name**	**Signal Name**	**Signal Name**
1	DCD	Tx-	DATA-
2	RxD	Tx+	DATA+
3	TxD	Rx+	NC
4	DTR	Rx-	NC
5	GND	NC	NC
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.3.2 Audio connector

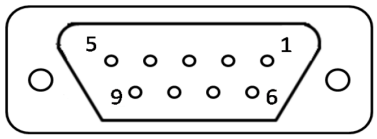


Table 2.6: Audio Connector Pin Definition

Pin	Signal Name	Pin	Signal Name
1	MICR	6	LOUTR
2	GND_AUD	7	GND_AUD
3	GND_AUD	8	Front_JD
4	MIC_JD	9	LOUTL
5	MICL		

2.3.3 Digital I/O connector

ITA-5831 provides 1 x 8-bits DIO with DB9 type (4DI, 4 DO).

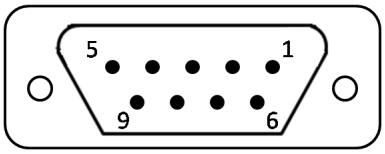


Table 2.7: Digital I/O Connector Pin Definition

Pin	Signal Name	Pin	Signal Name
1	GPI1	5	GPO1
2	GPI2	6	GPO2
3	GPI3	7	GPO3
4	GPI4	8	GPO4
9	GND		

2.3.4 USB connector

ITA-5831 provides total 2 x USB3.0 with Type A connector and 1 x USB2.0 with M12 A-code female connector. The USB interface can be disabled in the system BIOS setup.

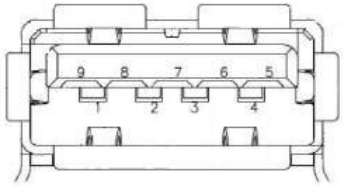


Table 2.8: USB3.0 Connector Pin Definition

Pin	Signal Name	Pin	Signal Name
1	+V5(VCC)	6	StdA_SSRX+
2	D-	7	GND_DRAIN
3	D+	8	StdA_SSTX-
4	GND	9	StdA_SSTX+
5	StdA_SSRX-		

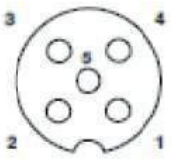


Table 2.9: USB2.0 connector Pin Definition

Pin	Signal Name	Pin	Signal Name
1	+5V	4	NC
2	D-	5	GND
3	D+		

2.3.5 Ethernet

ITA-5831 provides 3 x 10/100/1000M Ethernet with M12 x-coded.

Table 2.10: Ethernet Connector Pin Definition

Pin	Signal Name	Pin	Signal Name
1	MDI0+	5	MDI3+
2	MDI0-	6	MDI3-
3	MDI1+	7	MDI2-
4	MDI1-	8	MDI2+

2.3.6 Power Input

Table 2.11: Power Connector Pin Definition

Pin	Signal Name	Pin	Signal Name
1	PWR	3	GND
2	PWR	4	NC

2.3.7 LED Indicators for System Status

LEDs on the panel are used to indicate system health and active status. For detailed information of LED definition, please refer to the table below.

Item	LED	Status	Color	Description
1	PWR	On	Green	System power is on and system is safe.
		Off		
2	HDD	On	Yellow	Data receiving/transmitting
		Off		No active
3	FAULT_SYS	On	Red	System fault alarm
		Off		
4	Battery	On		Charge: Yellow Discharge: Red Low power alarm: Red blinking Full charge: No LED lighting
		Off		

Chapter 3

System Setup

Sections include:

- Installing mini-PCIe card and mSATA on mainboard
- Installing ITA-EM easy-swap modules
- Installing RTC battery
- Installing antennas

3.1 Introduction

The following procedures instruct you how to install all modules into the ITA-5831 system.

3.1.1 Installing m-SATA

ITA-5831 reserves 1 m-SATA slot on the mainboard and 3 mini-PCIe slot on the carrier board.

Figure 3.1 Installing mini-PCIe and m-SATA

1. Loosen the handscrews and pull out dual-SSD module from the front panel.
2. Open the top cover.
3. Loosen the screws to remove the dual-SSD bracket. Remove the carriage bracket for the easy-swap module.
4. Insert the mSATA or mini-PCIe, then lock it with 2 screws.

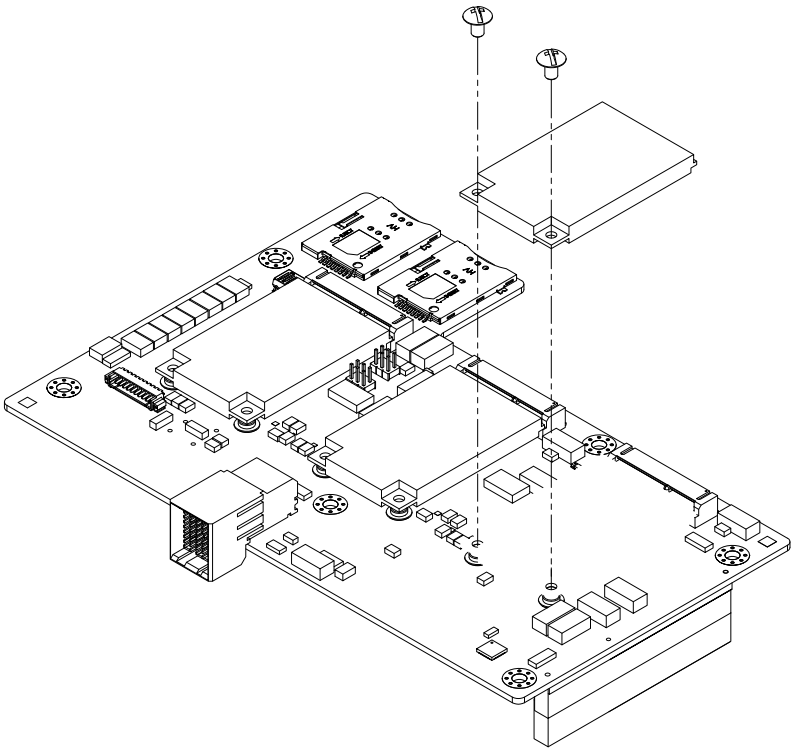


Figure 3.2 Installing mini-PCIe

3.1.2 Installing SSD

ITA-5831 contains 1 x Dual-SSD module inside. To install the SSD, pull out the SSD bracket and lock it with 4 screws.

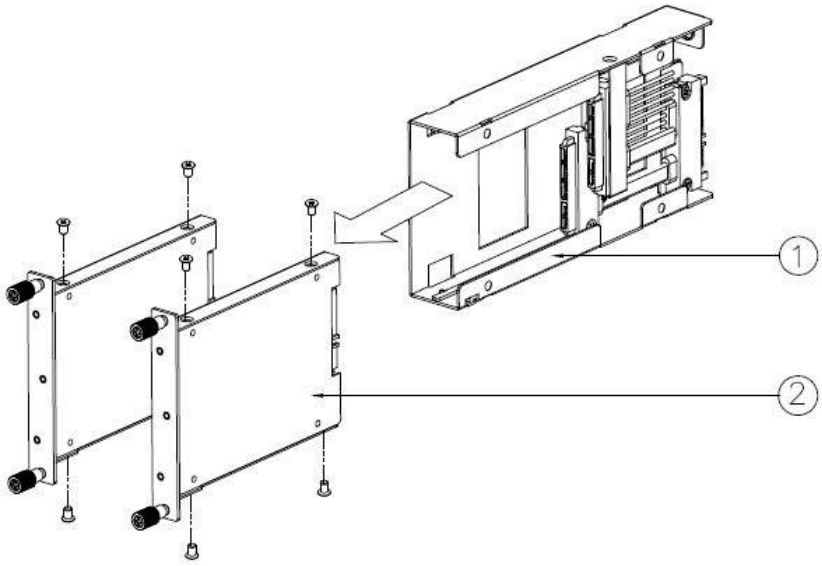


Figure 3.3 Installing SSD (1)

1. Loosen the hand screws and pull out the dual-SSD module on the front panel.
2. Install the SSD on the bracket and lock the SSD with 4 screws on both sides.

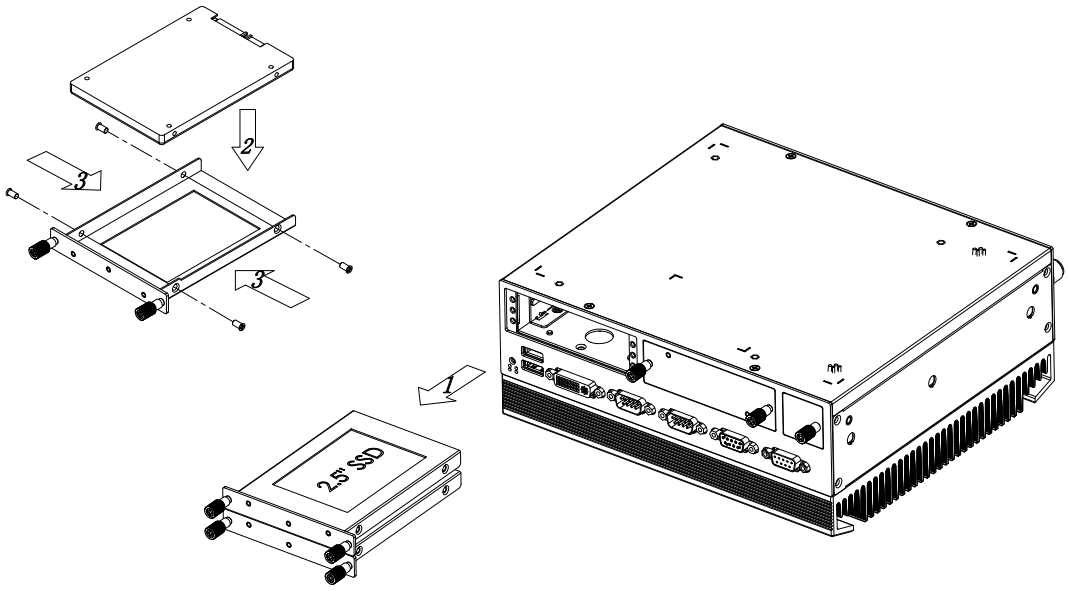


Figure 3.4 Installing SSD module (2)

3.1.3 Installing ITA-EM Easy-Swap modules

ITA-5831 reserves a blank bracket for an easy-swap module to extend your extra I/O requirements. A dual-SSD module can be removed and changed for other easy-swap modules.

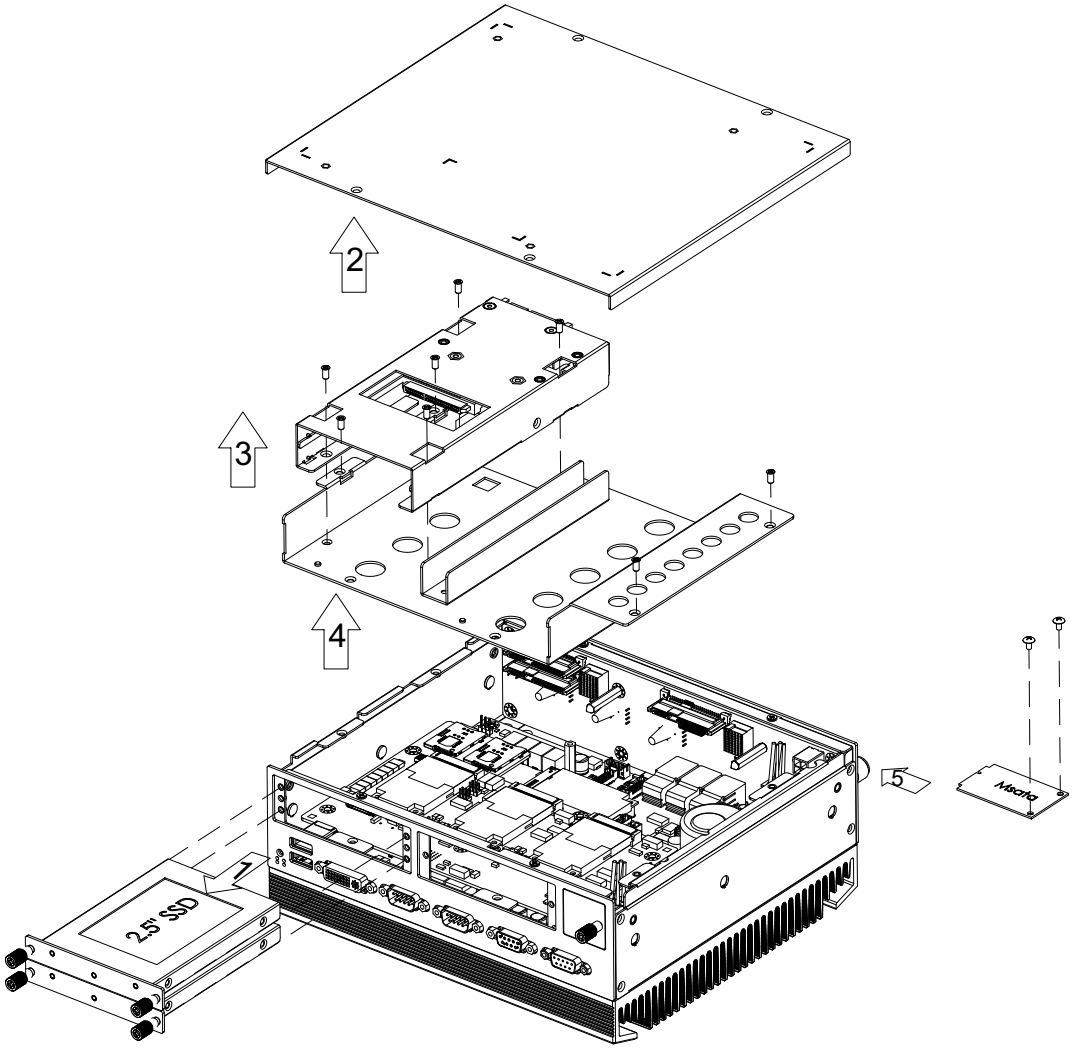


Figure 3.5 Installing Easy-Swap modules (1)

1. Loosen the handscrews and remove the blank bracket.
2. Insert the ITA-EM module and lock the handscrews.

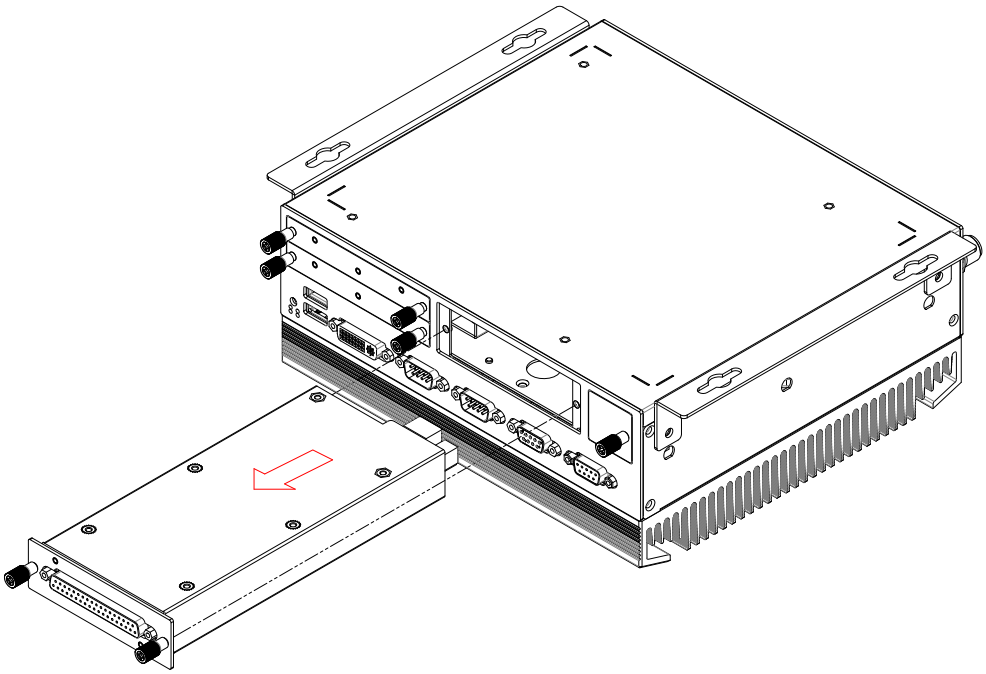


Figure 3.6 Installing Easy-Swap modules (2)

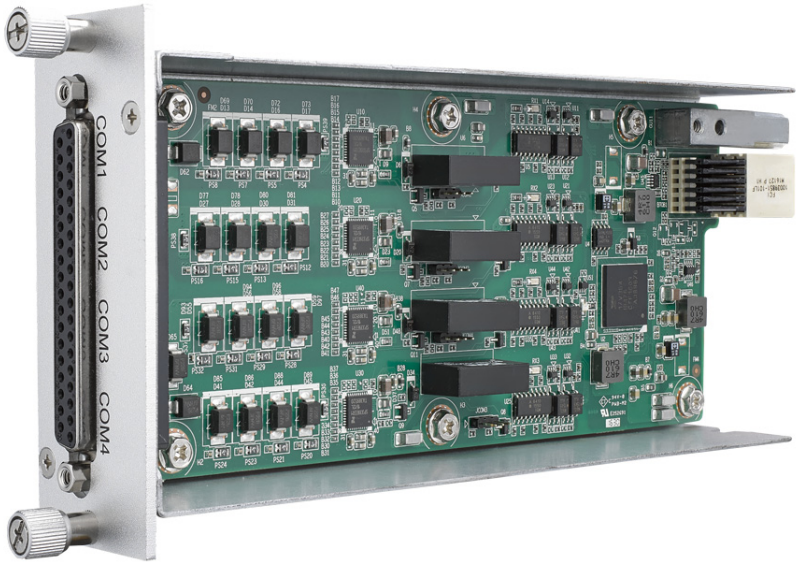


Figure 3.7 COM module (ITA-EM-SR61-001AE)

3.1.4 Installing RTC

ITA-5831 RTC battery is mounted on the front panel.

1. Open the RTC cover.
2. Insert the RTC battery to the holder and plug in the cable.
3. Lock the RTC cover.

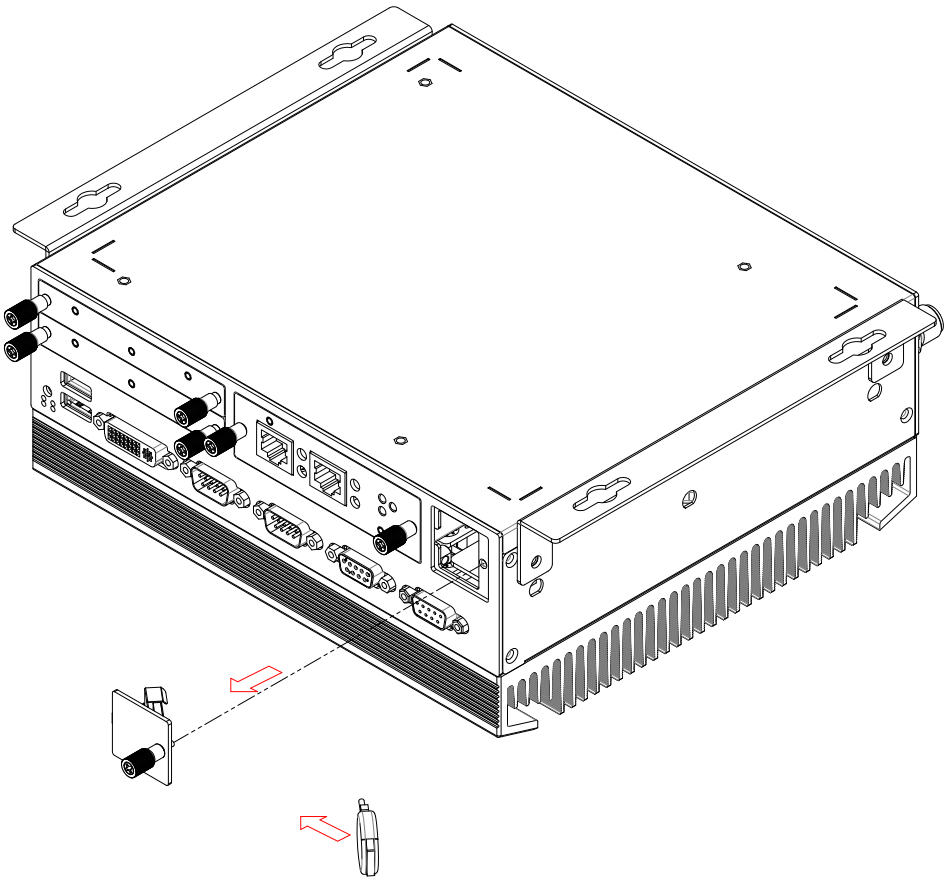


Figure 3.8 Installing RTC

3.1.5 Installing Antennas

IT-5231 reserves antenna holes on the front panel.

1. Loosen the handscrews and pull out the dual-SSD module from the front panel.
2. Open the top cover.
3. Loosen the screws to remove the dual-SSD bracket. Remove the carriage bracket for the easy-swap module. Insert the mini-PCIe, then lock it with 2 screws.
4. Install the antennas on both side of the chassis.

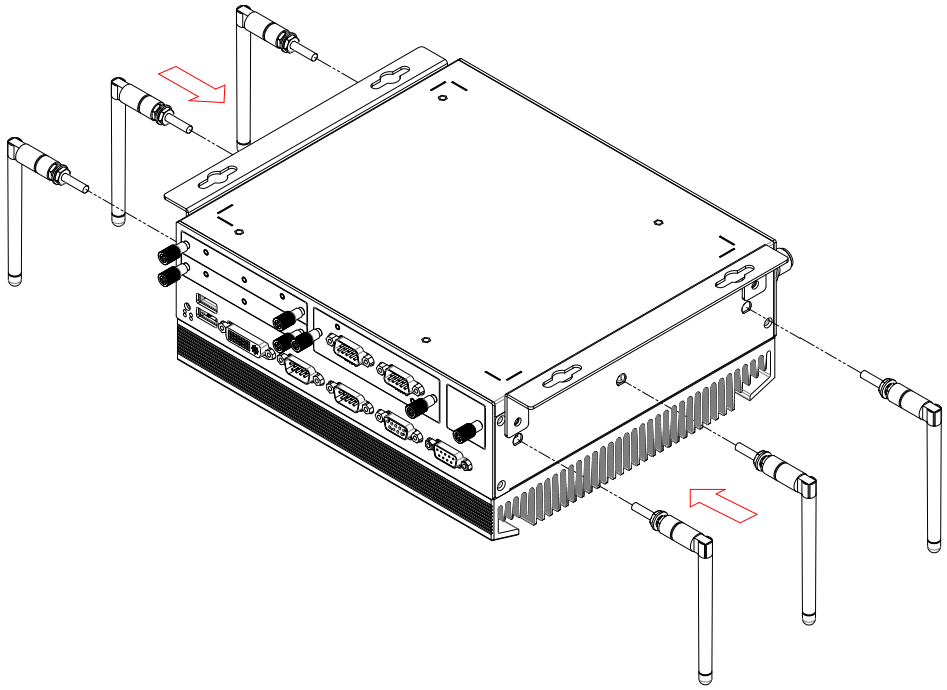


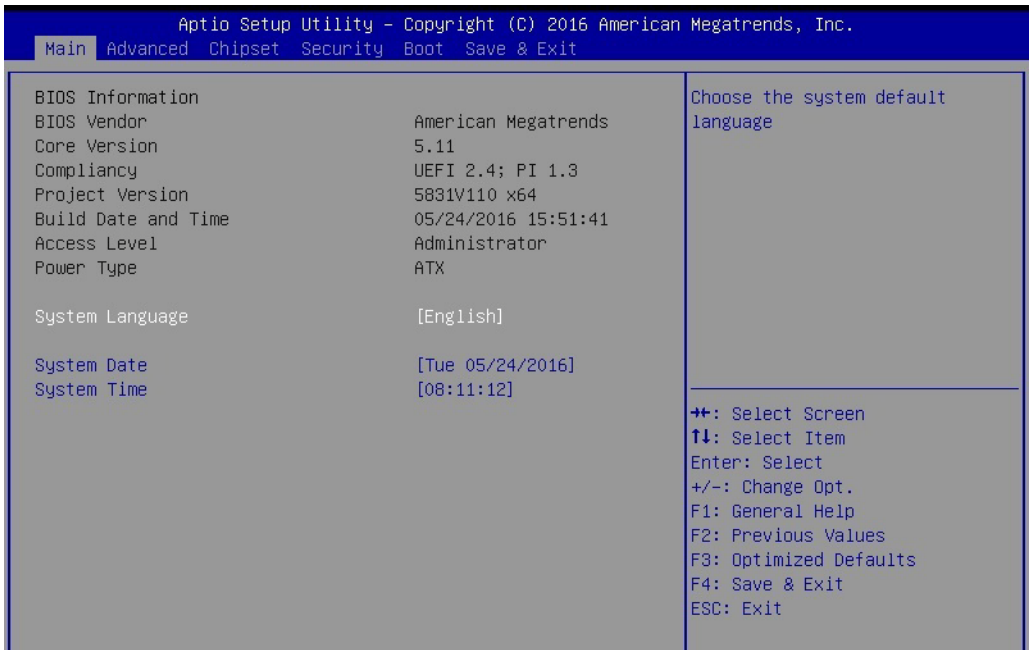
Figure 3.9 Installing antennas

Chapter 4

BIOS Setting

4.1 Introduction

This chapter introduces how to configure BIOS for ITA-5831 series.With the AMI-BIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter describes the basic navigation of the ITA-5831 setup screens.

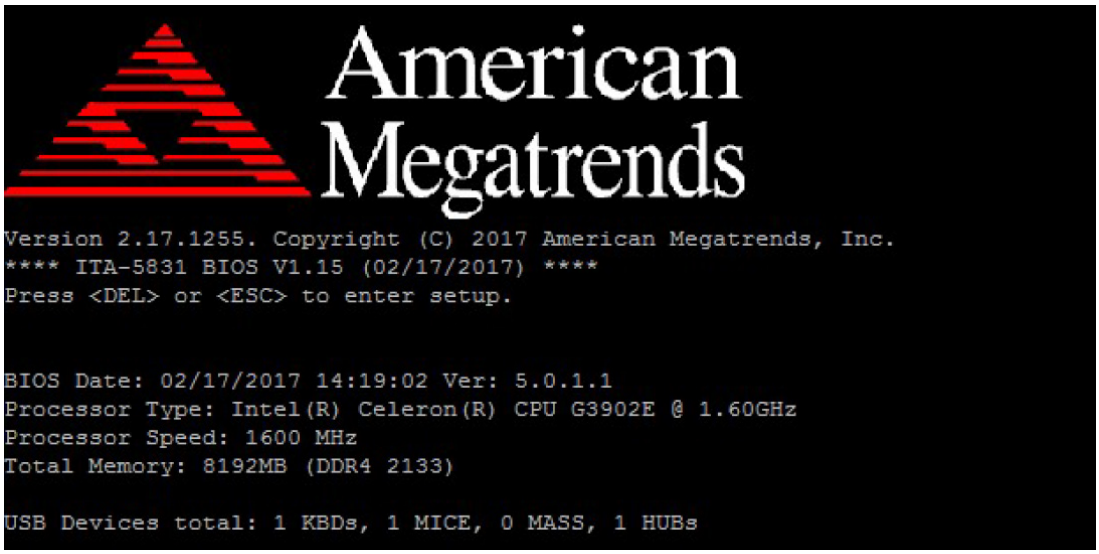


AMI's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed up CMOS, so it retains the Setup information when the power is turned off.

4.2 Entering Setup

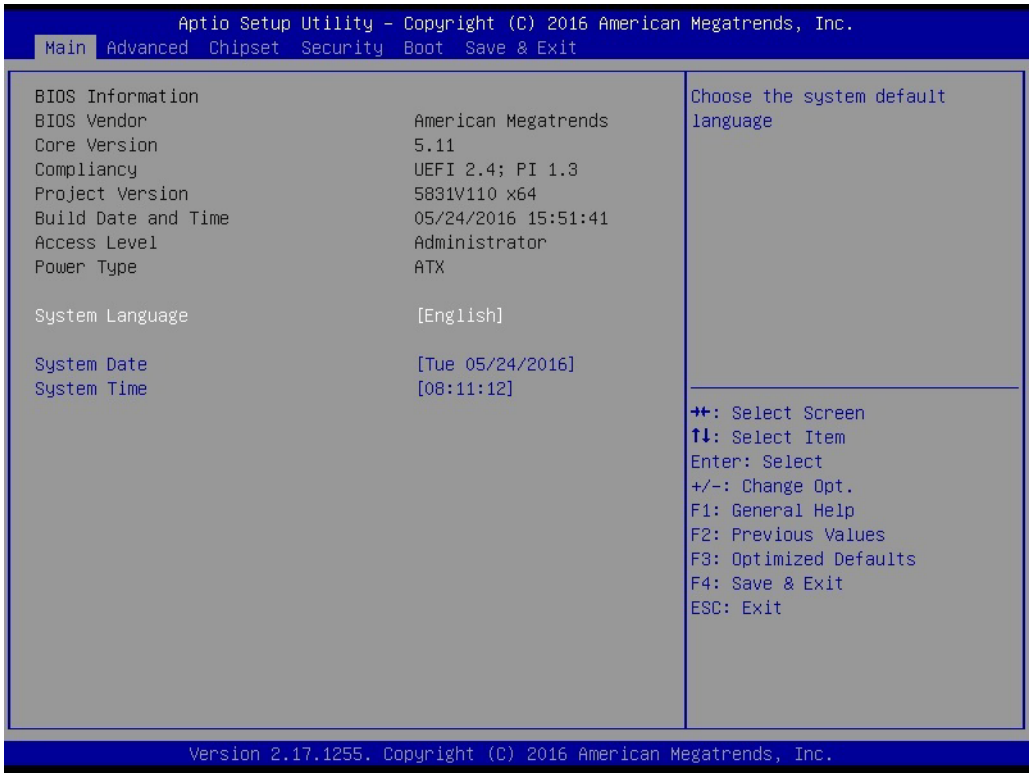
Turn on the computer to enter POST screen, and BIOS and CPU information will be shown.

Press <DEL> and you will immediately be allowed to enter Setup.



4.3 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



The Main BIOS setup screen has two main parts. The part in left displays all the options that can be configured. Grayed-out options cannot be configured, and options in blue can. The right part displays the explanation of the shortcut keys.

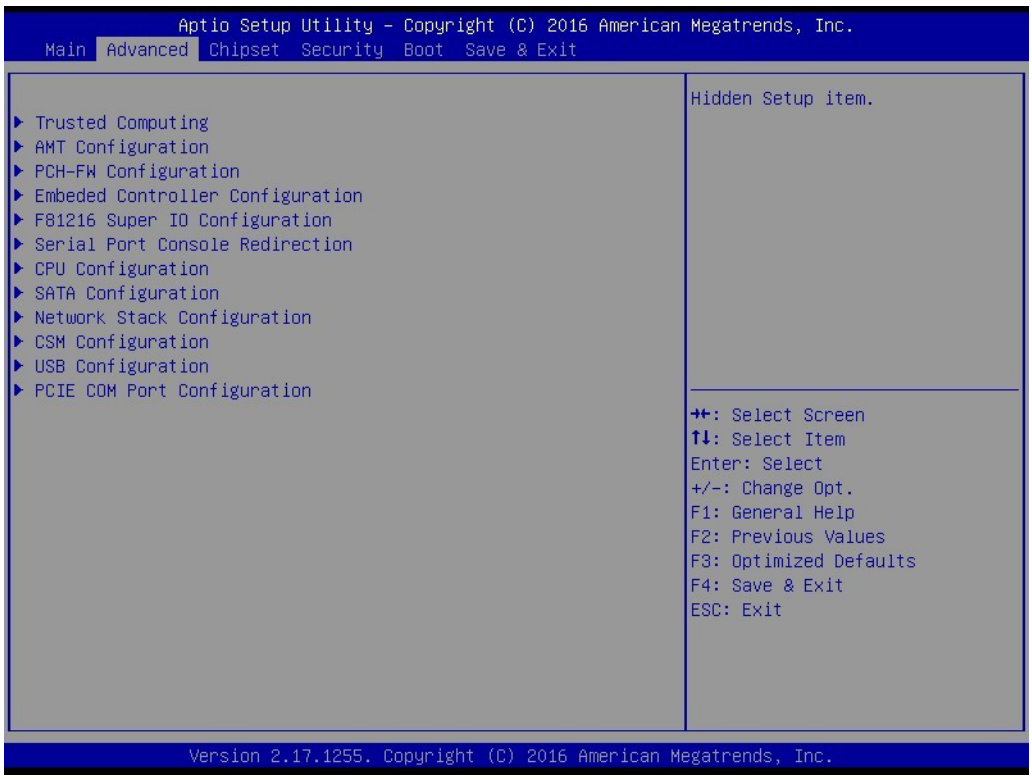
Above the key explanations is an area reserved for a text message. When an option is selected in the left part, it is highlighted in white, and the information of this option will accompany it.

- **System Time/System Date**

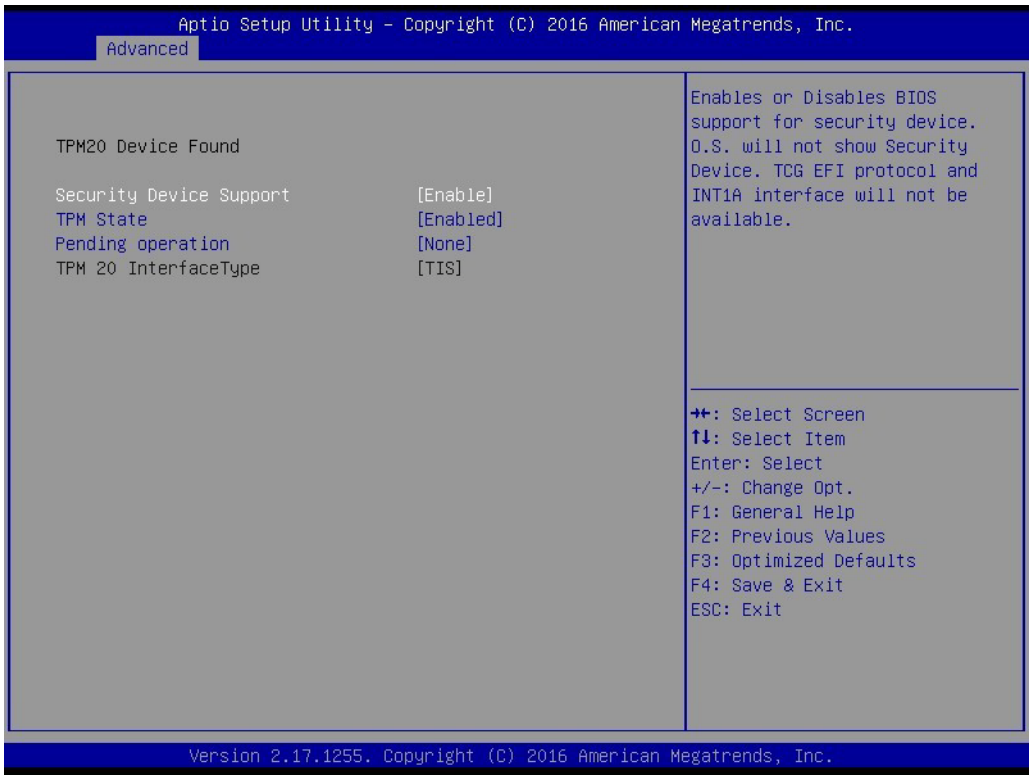
  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard.Press the <Tab> key or the <Arrow> keys to move the next fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

4.3.1 Advanced BIOS Setup

Select the Advanced tab from the ITA-5831 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this page. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.



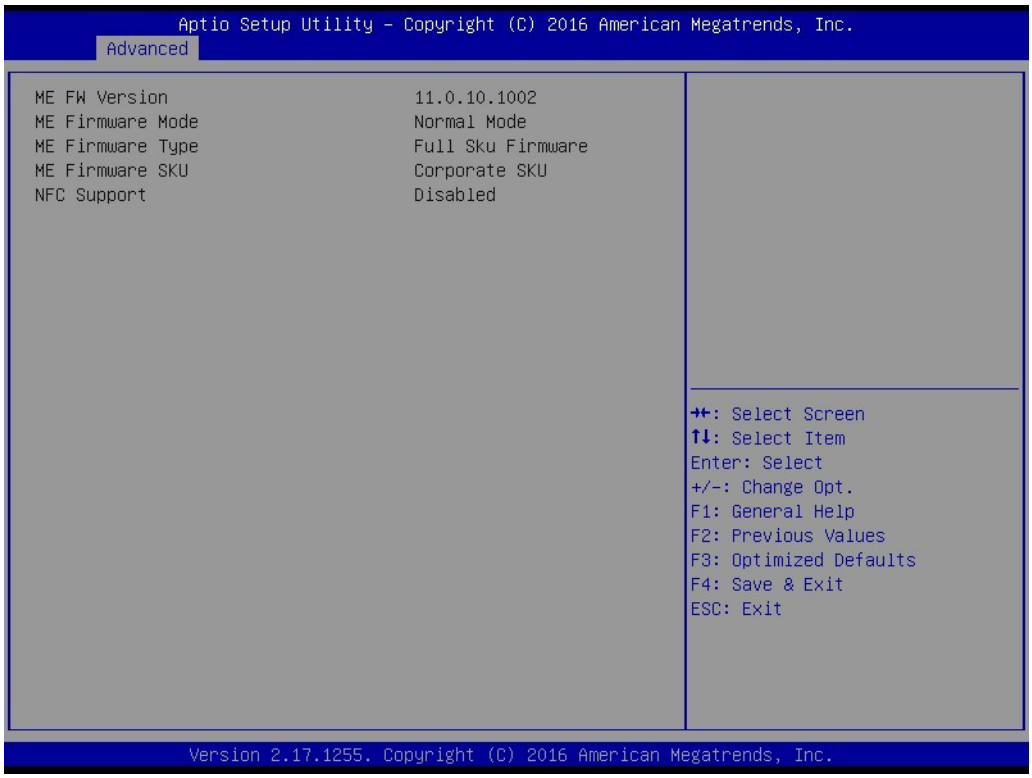
4.3.1.1 Trusted Computing



- **Security Device Support:**
  Enable/Disable BIOS support for security device. The default setting is [Enable].
- **TPM state:**
  Enable/disable security device. The default setting is [Enable].
- **Pending operation:**
  Schedule an operation for the security device. TPM can be clear or none. The default setting is [None]

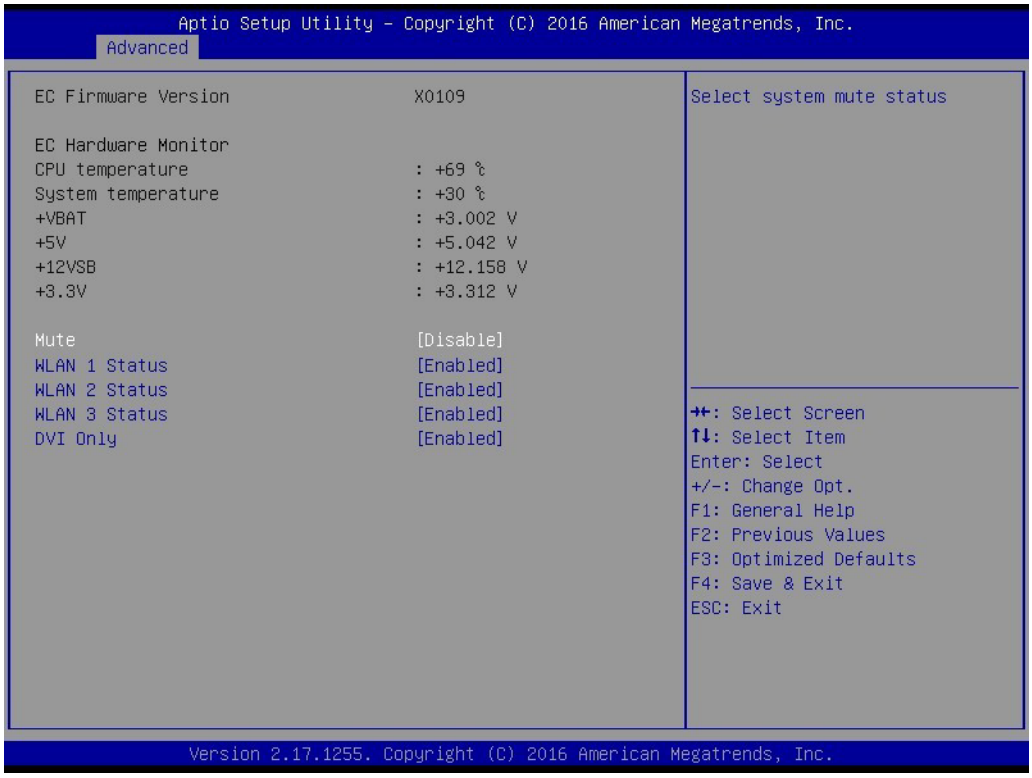
4.3.1.2 PCH-FW Configuration

This page shows the version, mode, type, SKU of ME firmware which build-in BIOS.



4.3.1.3 Embedded Controller Configuration

This page shows a part of hardware information which accessed by EC. The user can get the temperature or voltage to analyze the status of system.

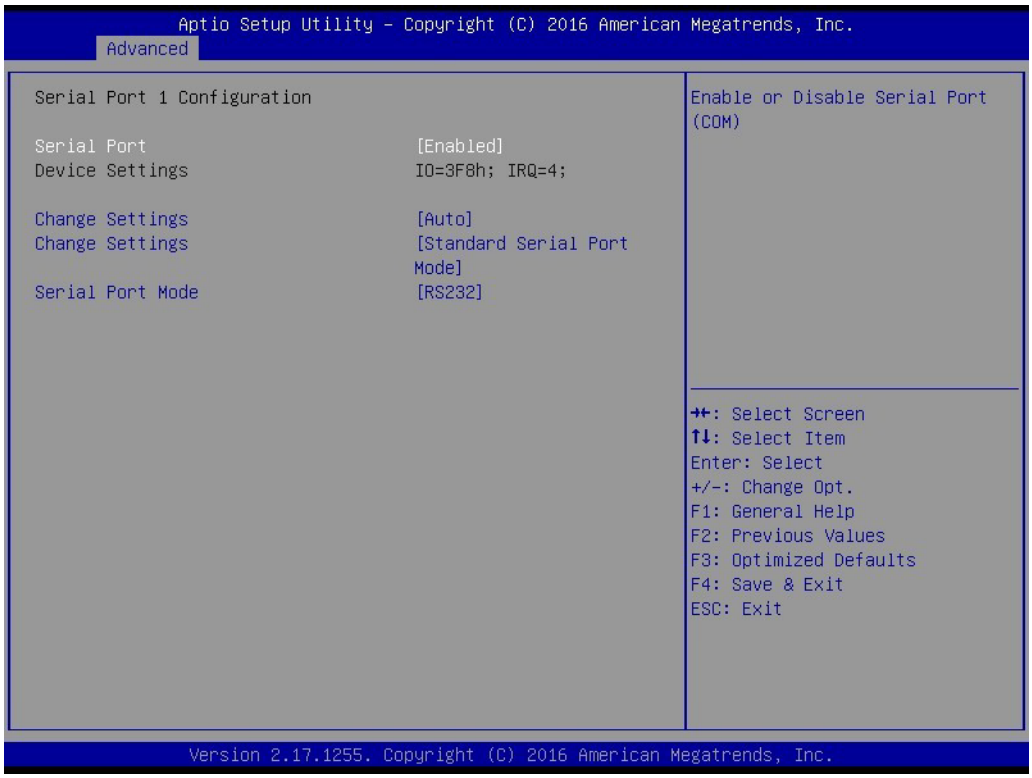


- **Mute:**
  Control the system voice. The default settings is [Disable].
- **WLAN 1/2/3 Status:**
  Control the WLAN status. The default setting is [Enable].
- **DVI only:**
  If only the DVI device is connected, this setting can be set to [enable]. The default setting is [Disable].

4.3.1.4 F81216 Controller Configuration

The ITA-5831 support 2 serial ports. The user can configure the serial port in the sub-page. The serial port 60 is hardware reserved function, and the default setting is [disabled].

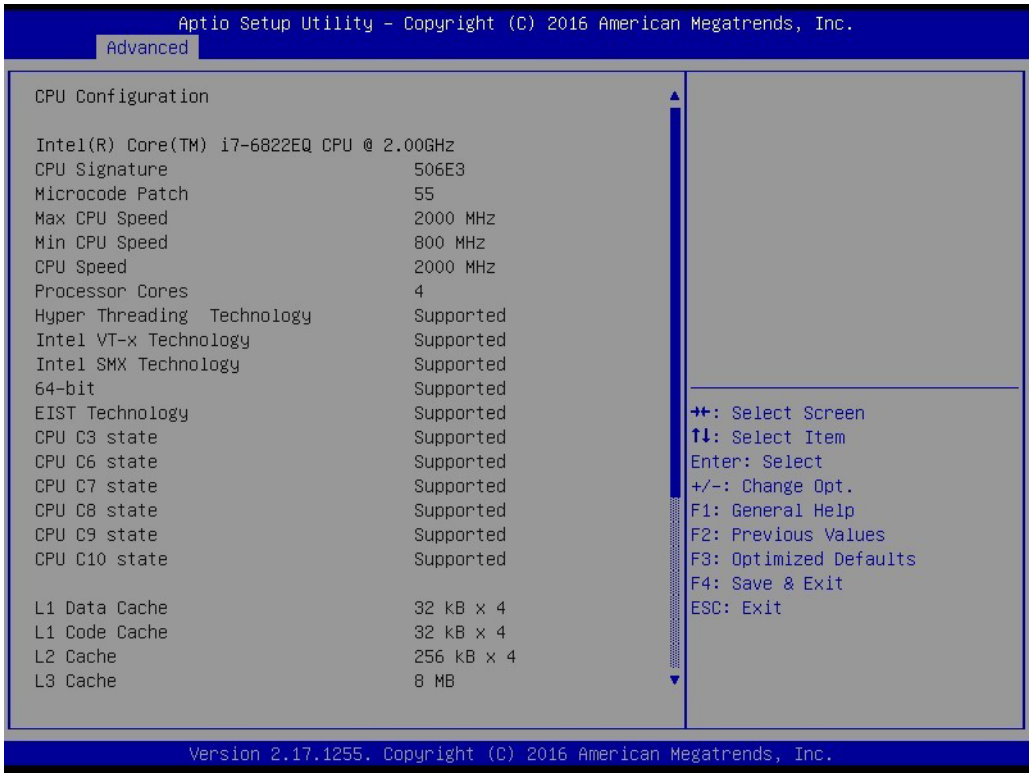
Serial Port 1/2 Configuration

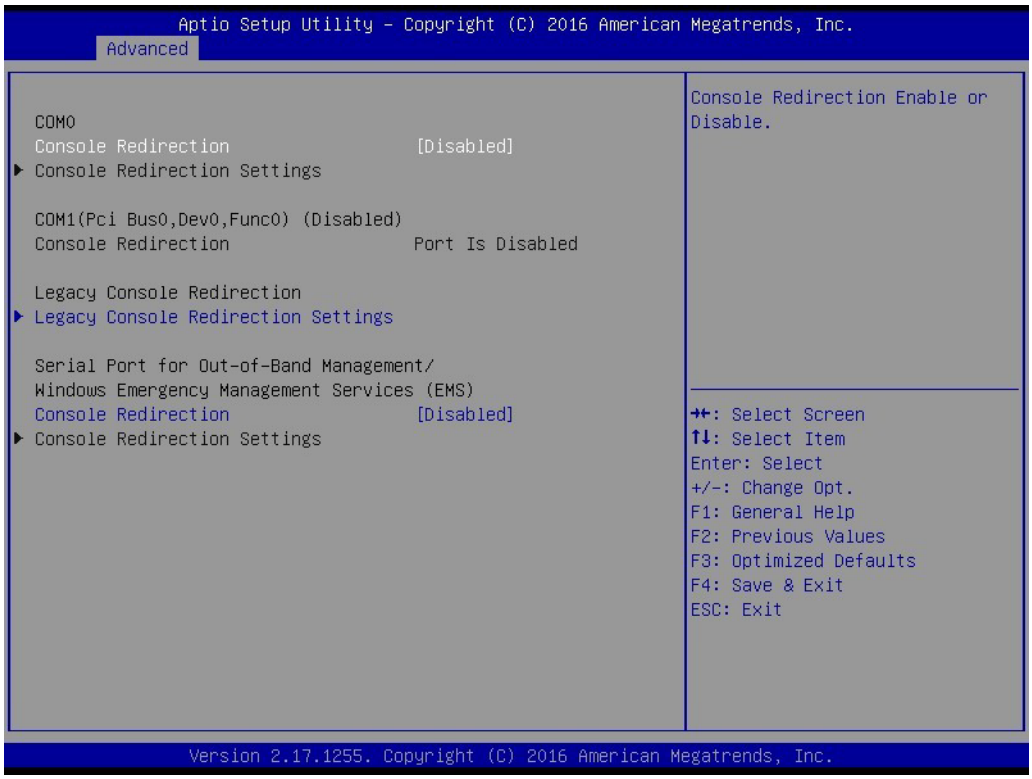


- **Serial Port**
  Enable /disable the serial port. The default setting is [Enabled].
- **Device Settings:**
  Display the IO port and IRQ number which the port used.
- **Change settings[1]:**
  Select an optimal settings for the serial port (IO port and IRQ). The default setting is [Auto].
- **Change settings[2]:**
  Select an optimal settings for the serial port (Full/Half Duplex). The default setting is [standard Serial Port Mode].
- **Serial Port Mode:**
  Select serial port mode(RS232/RS485). The default setting is [RS232].

4.3.1.5 Serial Port Console Redirection

This page shows the console status. The user can configure the console settings in [Console redirection Settings].

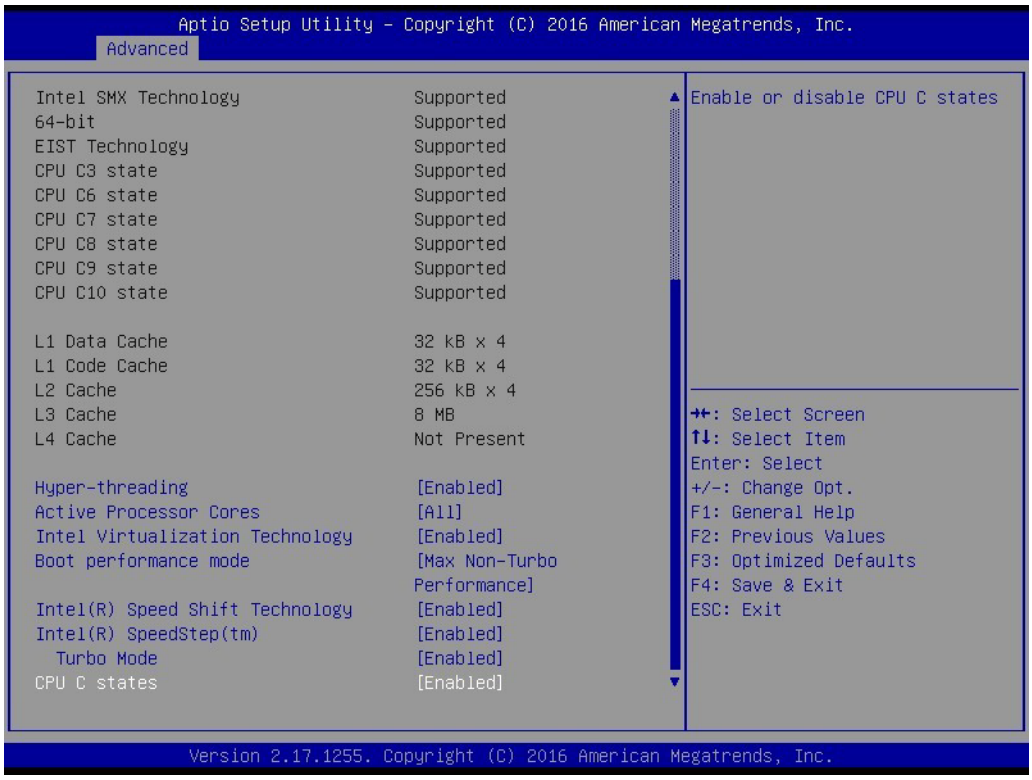




- **Console redirection:**
  Enable/disable console redirection function. The default settings is [disabled].
- **Console Redirection Settings:**
  When the function of console redirection is enabled, this BIOS sub-page can be entered. The settings specify how the host computer and the remote computer will exchange data. Both computers should have the same or compatible settings.
- **Legacy Console Redirection Settings:**
  This sub-page shows the legacy serial port number.

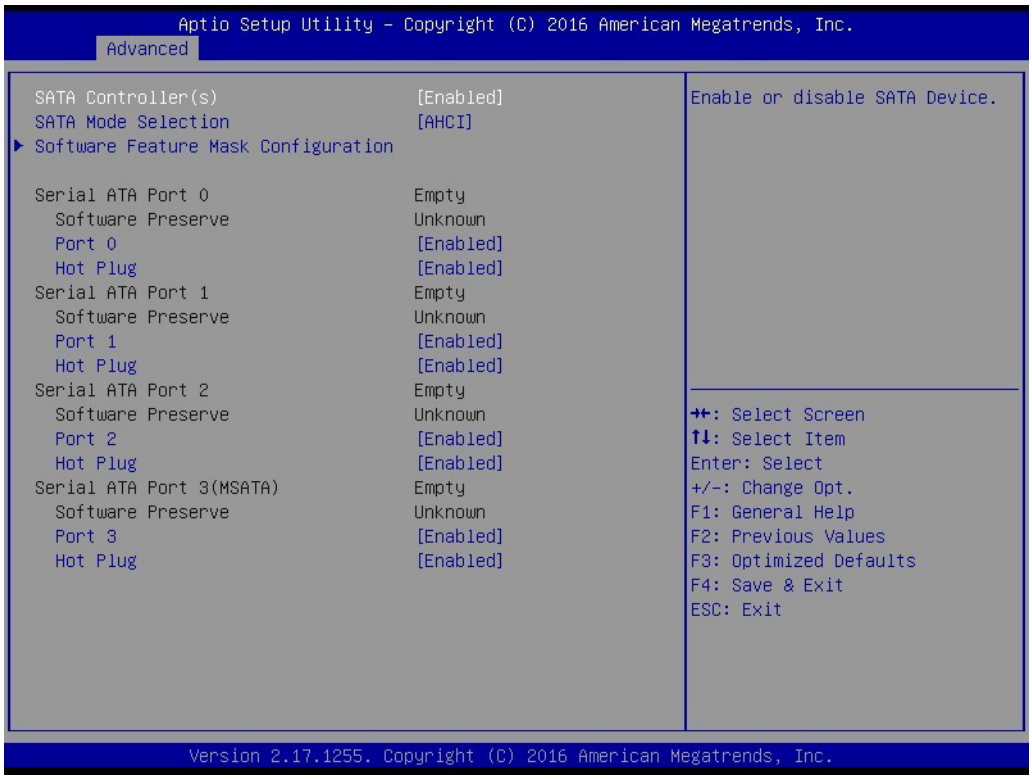
4.3.1.6 CPU Configuration

This page display the information of the system's CPU.



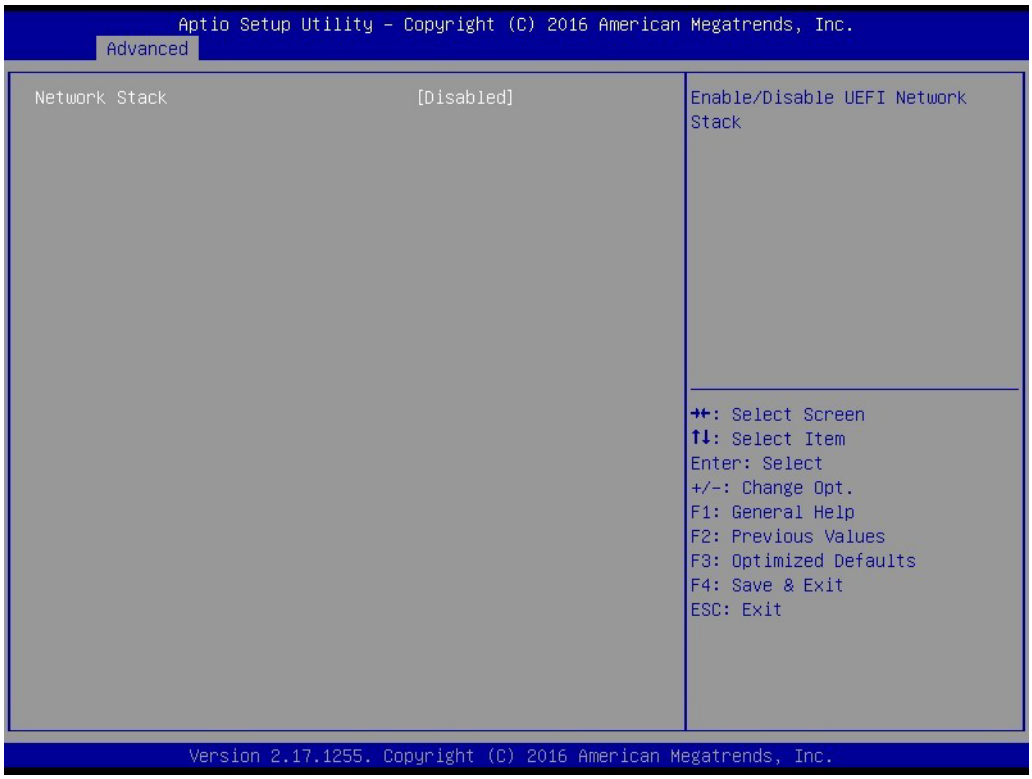
- **Hyper-threading**
  Enable/disable CPU hyper-threading function. The default setting is [Enabled].
- **Active Processor Cores**
  Select the number of cores to enable in each processor package. The default setting is [ALL].
- **Intel Virtualization Technology**
  When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. The default setting is [Enabled].
- **Boot performance mode**
  Select the performance state that the BIOS will set before OS handoff. The default setting is [Max Non-Turbo Performance].
- **Intel(R) Speed shift Technology**
  Enable/disable allows more than two frequency ranges to be supported. The default setting is [Enabled].
- **CPU C sates**
  Enable/disable CPU C states. The default setting is [Enabled].

4.3.1.7 SATA Configuration



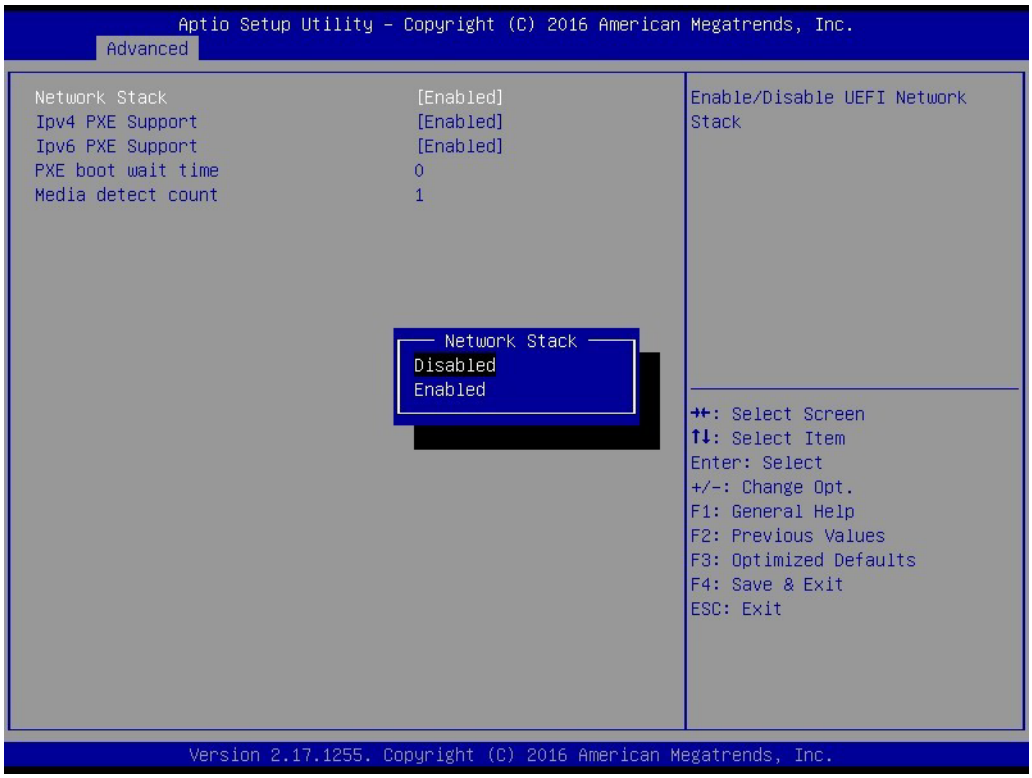
- **SATA Controller(s):**
  Enable/disable SATA controllers. The default setting is [Enabled].
- **SATA Mode Selection**
  Determines how SATA controllers operate, AHCI or RAID can be chosen. The default setting is [AHCI].
- **SATA Port 0/1/2/MSATA**
  Enable/disable SATA ports. The default setting is [Enabled].
- **Hot plug**
  Designates this port as hot pluggable. The default setting is [Enabled].

4.3.1.8 Network Stack Configuration



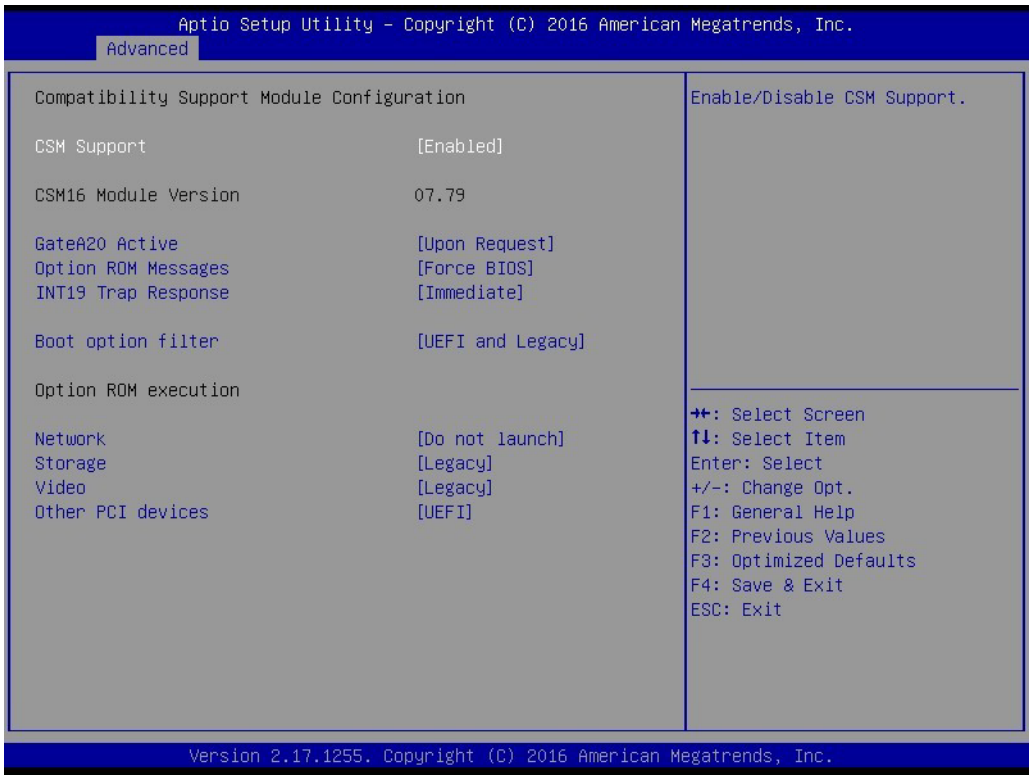
- **Network Stack**
  Enable/Disable UEFI Network stack. The default setting is [Disabled].

When enable Network stack, the followed picture will be shown:



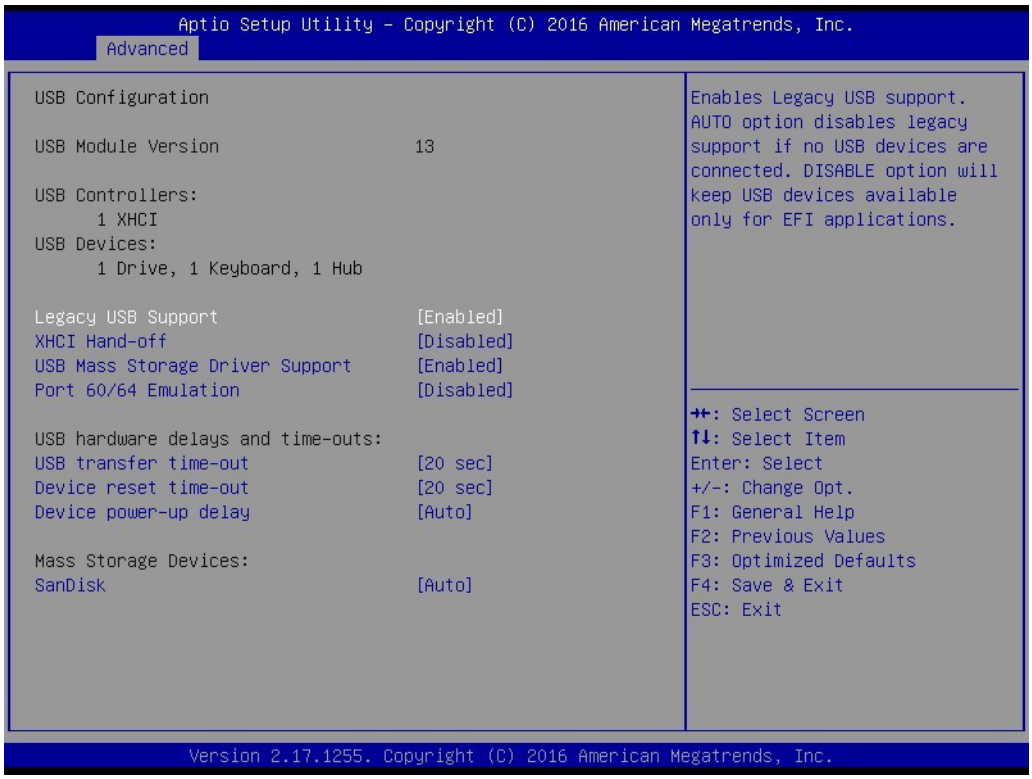
- **Ipv4 PXE Support:**
  Enable/Disable IPV4 PXE support. If disabled, IPV4 PXE boot option will not be created.
- **Ipv6 PXE Support:**
  Enable/Disable IPV6 PXE support. If disabled, IPV6 PXE boot option will not be created.
- **PXE boot wait time:**
  Set wait time to press ESC key to abort the PXE boot.
- **Media detect count:**
  Set the number of times presence of media will be checked.

4.3.1.9 CSM Configuration



- **CSM Support**
  Enable/disable CSM support. The default setting is [Enabled].
- **GateA20 Active**
  [Upon Request]: GA20 can be disabled using BIOS services.
  [Always]: Do not allow disabling GA20.
- **Option ROM Messages**
  Set the display mode for option ROM.
- **INT19 Trap Response**
  BIOS reaction on INT19 trapping by option rom.
  [Immediate]: execute the trap right way
  [Postponed]: execute the trap during legacy boot.
- **Boot option filter**
  This option controls legacy/UEFI ROMs priority.
- **Network**
  Controls the execution of UEFI and legacy PXE OpRom.
- **Storage**
  Controls the execution of UEFI and legacy Storage OpRom.
- **Video**
  Controls the execution of UEFI and legacy Video OpRom.
- **Other PCI devices**
  Determines OpRom execution policy for devices other than network, storage or video.

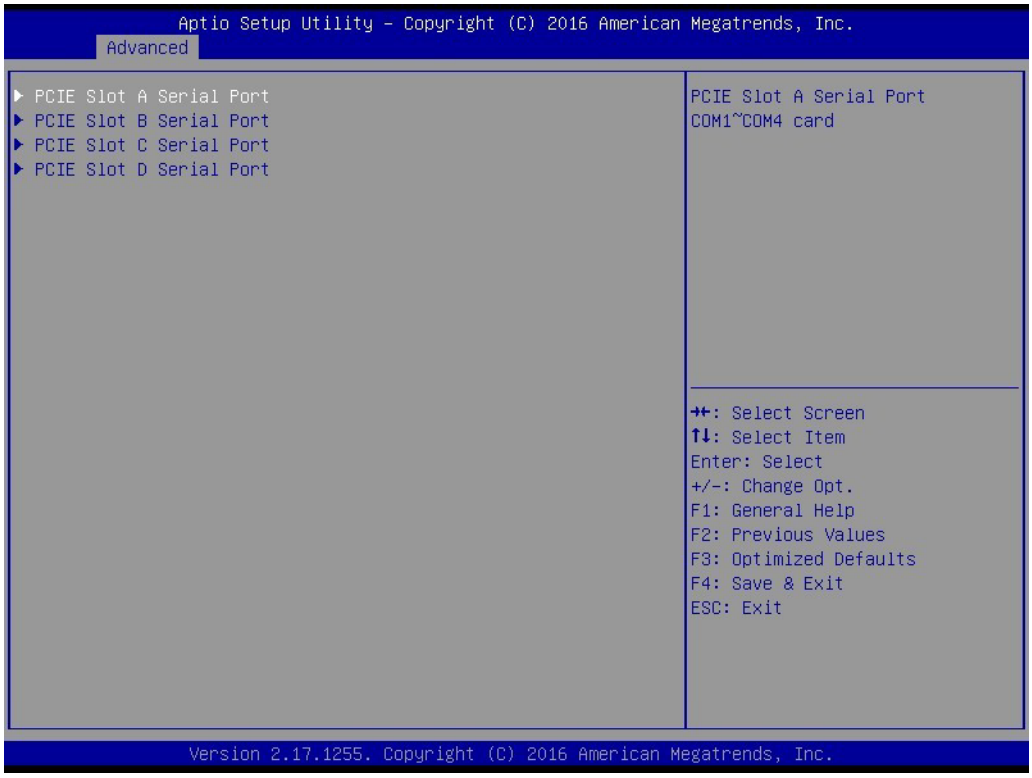
4.3.1.10 USB Configuration

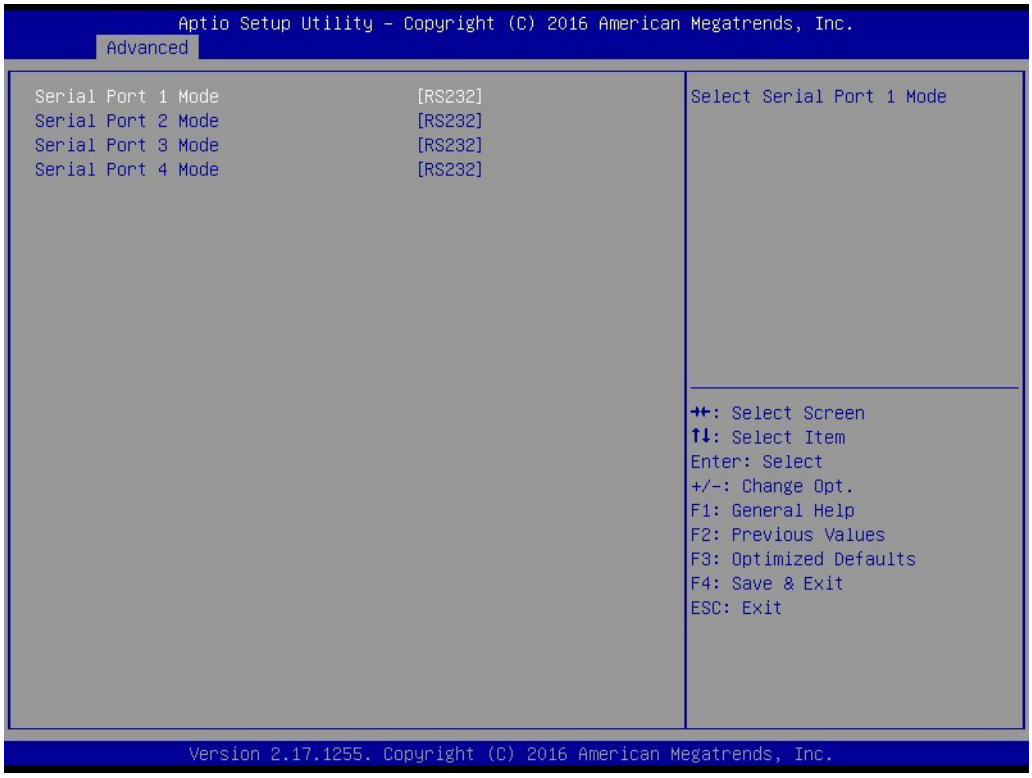


- **Legacy USB Support:**
  Enable/disable legacy USB support. The default settings is [enabled].
- **XHCI Hand-off**
  This is a workaround for OS without XHCI hand-off support. The XHCI ownership changes should be claimed by XHCI driver.
- **USB Mass Storage Driver Support**
  Enable/disable USB Mass Storage driver support.
- **Port 60/64 Emulation**
  Enable/disable I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OS.
- **USB transfer time-out**
  Set the time-out value for control, bulk, and interrupt transfers.
- **Device power-up delay**
  Set the time-out value for USB mass storage device start unit command.

4.3.1.11 PCIE COM Port Configuration

ITA-5831 Support 4 PCIE slot serial ports. The user can configure serial port in sub page.



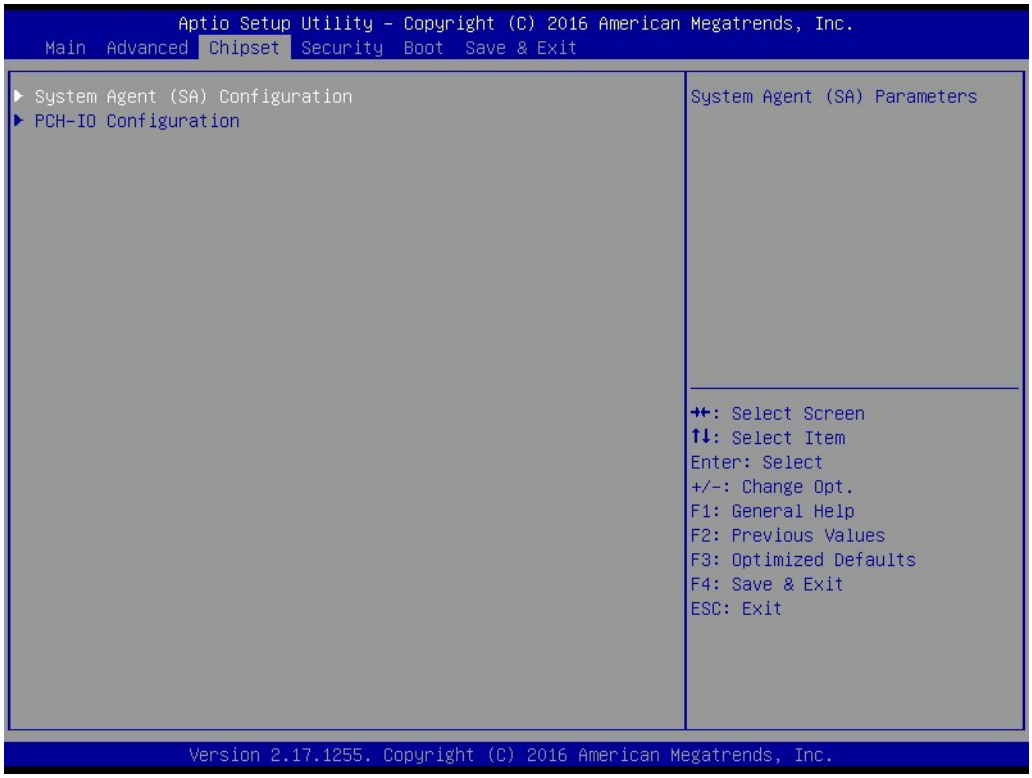


- **Serial Port 1/2/3/4 Mode:**

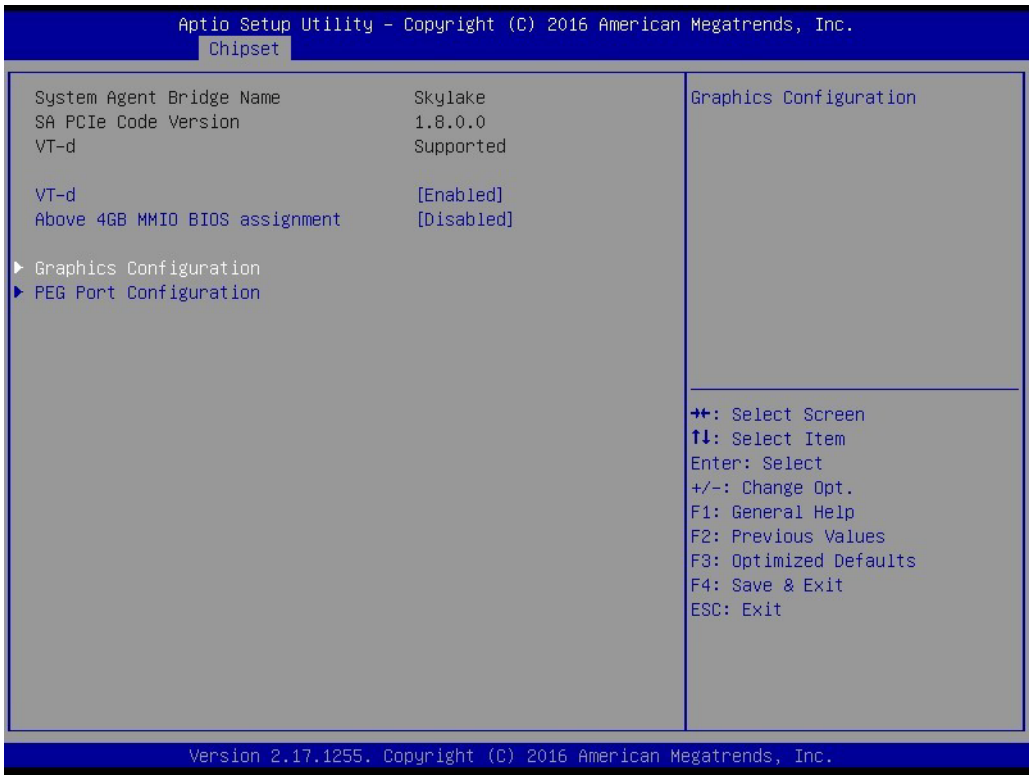
  Select serial ports mode. [RS232],[RS422],[RS485] can be selected. The default setting is [RS232].

4.3.2 Chipset Configurations

The user configures PCH and SA in the sub-page of chipset configurations.

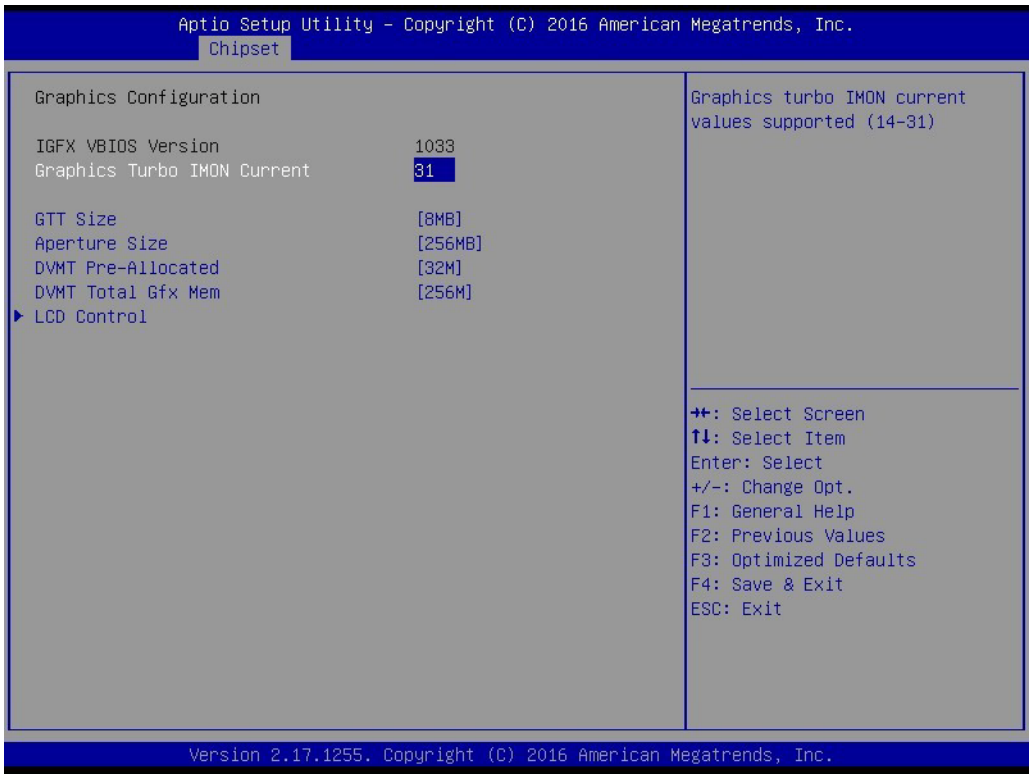


4.3.2.1 System Agent Configurations



- **VT-d**
  Enable/disable VT-d function.
- **Above 4GB MMIO BIOS assignment**
  Enable/disable above 4GB MMIO BIOS assignment. This is disabled by automatically when Aperture size is set to 2048MB.
- **Graphics Configuration**
  Configure graphics settings. Please refer 4.5.1.1.
- **PEG Port Configuration**
  Configure PEG ports settings. Please refer 4.5.1.2.

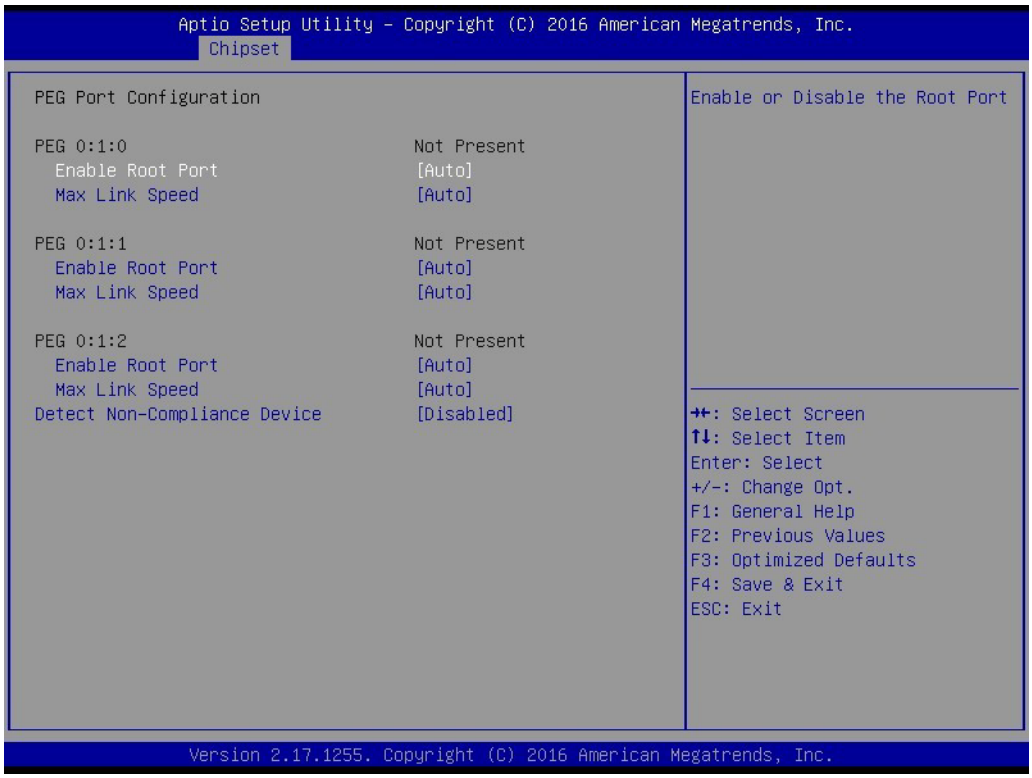
Graphics Configuration



- **IGFX VBIOS Version**
  Displays the current VBIOS version.
- **Graphics Turbo IMON Current**
  Set the graphics turbo IMON current values supported(14-31).
- **GTT size**
  Select the GTT size.
- **Aperture size**
  Select the aperture size. If 2048MB aperture size is selected, please disable CSM support.
- **DVMT Pre-Allocated**
  Select DVMT 5.0 Pre-Allocated (Fixed) Graphics memory size used by the Internal Graphics Device.
- **DVMT Total GFX Mem**
  Select DVMT 5.0 total Graphics memory size used by the Internal Graphics Device.
- **LCD control**
  Please refer the next page.

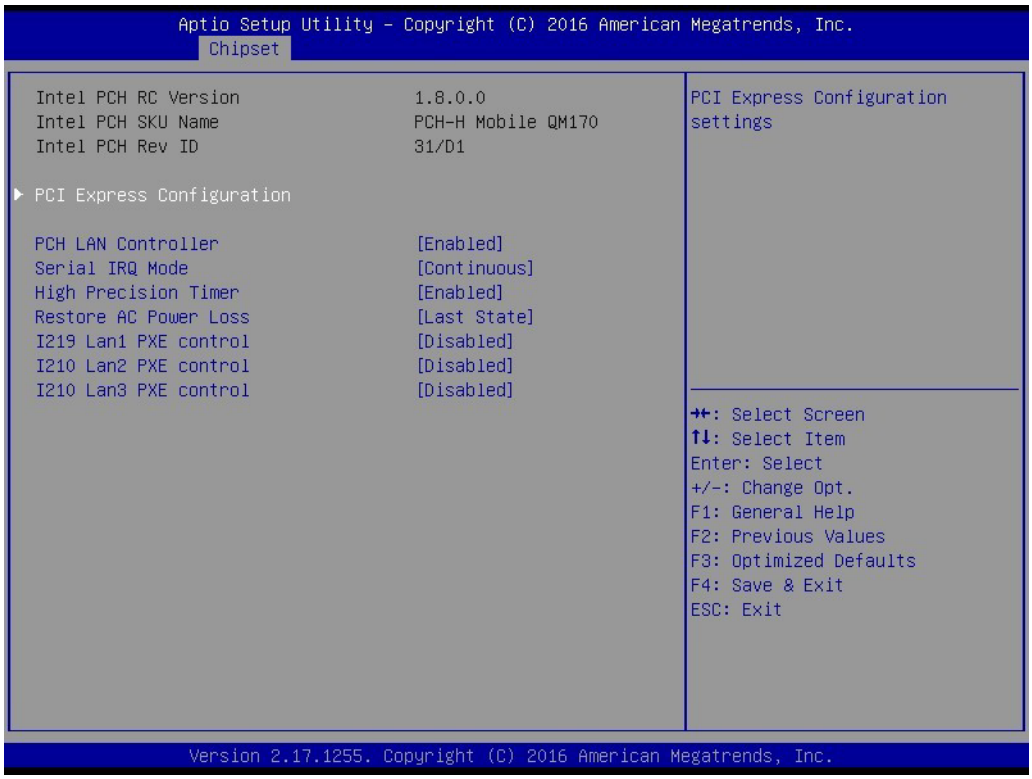
- **Primary IGFX Boot Display**
  Select the video device which will be activated during POST. Secondary boot display selection will appear based on your selection. ITA-5831 supports HDMI,DVI, eDP panel and VGA.
- **eDP LVDS Panel Type**
  Select ITB-172 LCD panel type.
- **Panel Scaling**
  Select the LCD panel scaling option used by the internal graphics device.
- **Backlight Control**
  Control backlight type.
- **Spread Spectrum clock chip**
  Set the type of spread spectrum clock.
  [Hardware]: Spread is controlled by chip
  [Software]: Spread is controlled by BIOS
- **Active LFP**
  Configure LFP usage.
- **Panel Color Depth**
  Select the LFP color depth.

PEG Port Configuration



- **Enable Root Port**
  Enable/disable the root port.
- **Max Link Speed**
  Configure PEG port max link speed.
- **Detect Non-Compliance Device**
  Detect non-compliance PCIE device in PEG port.

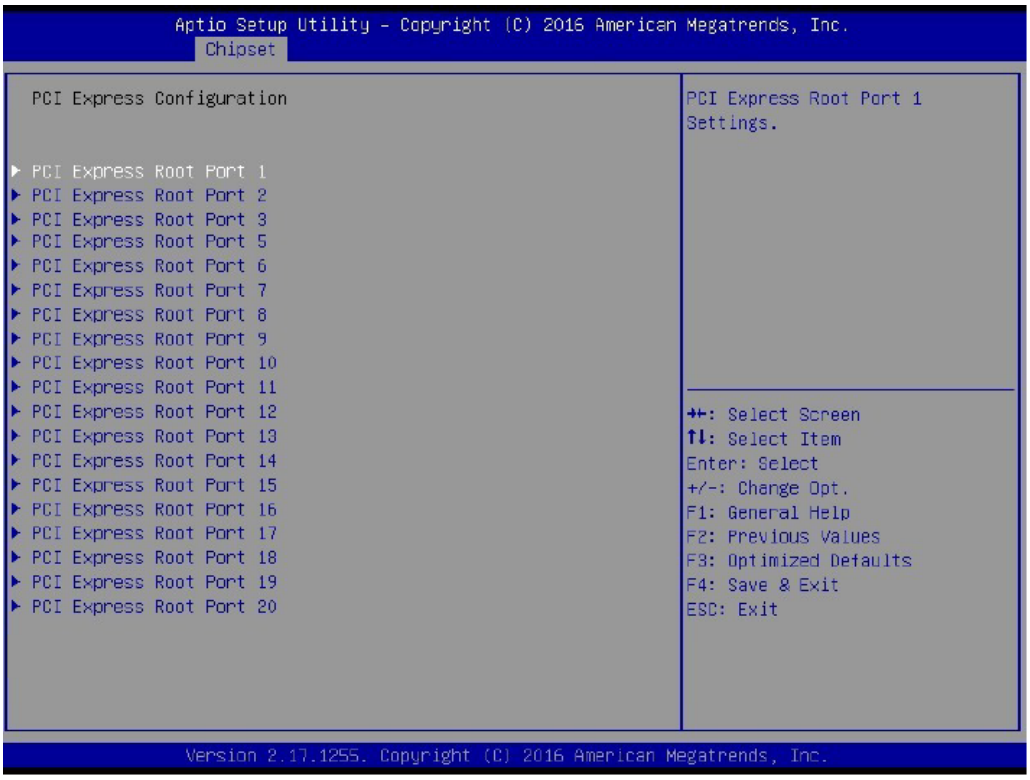
4.3.2.2 PCH-IO Configurations

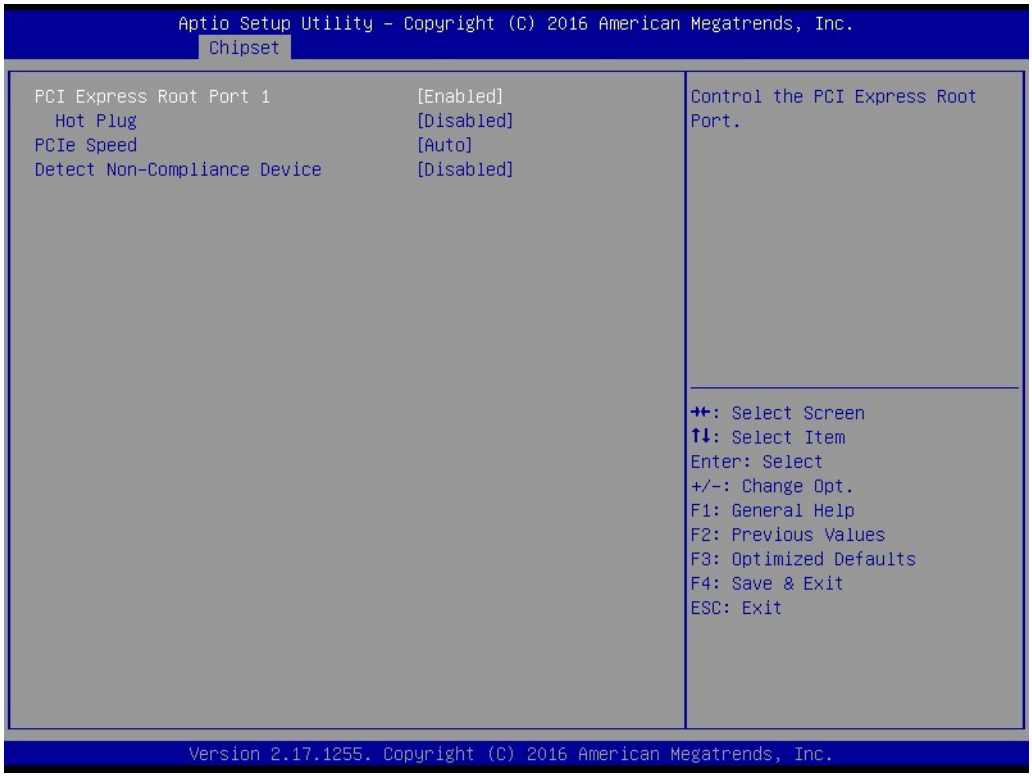


- **Intel PCH RC Version**
  Show the current Intel PCH RC version.
- **Intel PCH SKU Name**
  Show the current Intel PCH SKU name.
- **Intel PCH Rev ID**
  Show the current Intel PCH reversion id.
- **PCI Express Configuration**
  Please refer 4.5.2.1
- **PCH LAN Controller**
  Enable/disable onboard NIC.
- **Serial IRQ Mode**
  Configure serial IRQ mode.
- **High Precision Timer**
  Enable/disable the high precision event timer.
- **Restore AC Power Loss**
  Select AC power state when power is re-applied after a power failure.
- **I219/I210 LAN PXE Control**
  Enable/disable LAN PXE function.

PCI Express Configuration

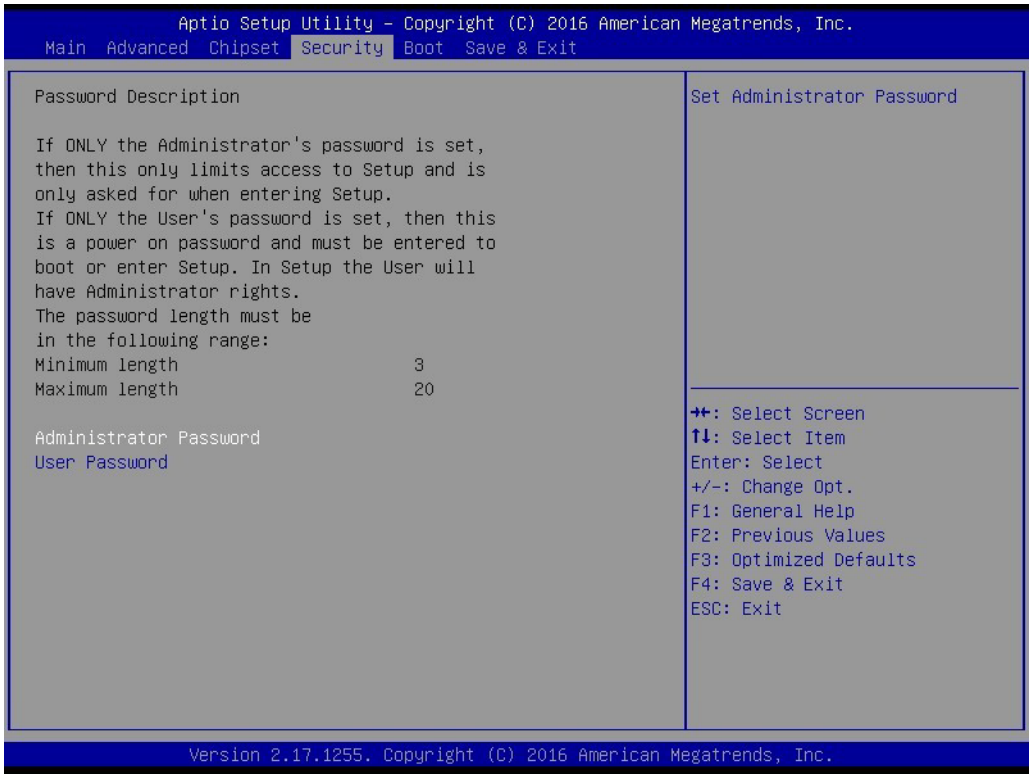
This page shows the PCH supports the PCIE root ports. Detailed configurations below.





- **PCI Express Root Port**
  Control the PCI Express root port.
- **Hot plug**
  Enable/disable PCI Express hot plug.
- **PCIe speed**
  Select PCI Express port speed.
- **Detect Non-Compliance device**
  Detect non-compliance PCI Express device. If enable, it will take more time at POST time.

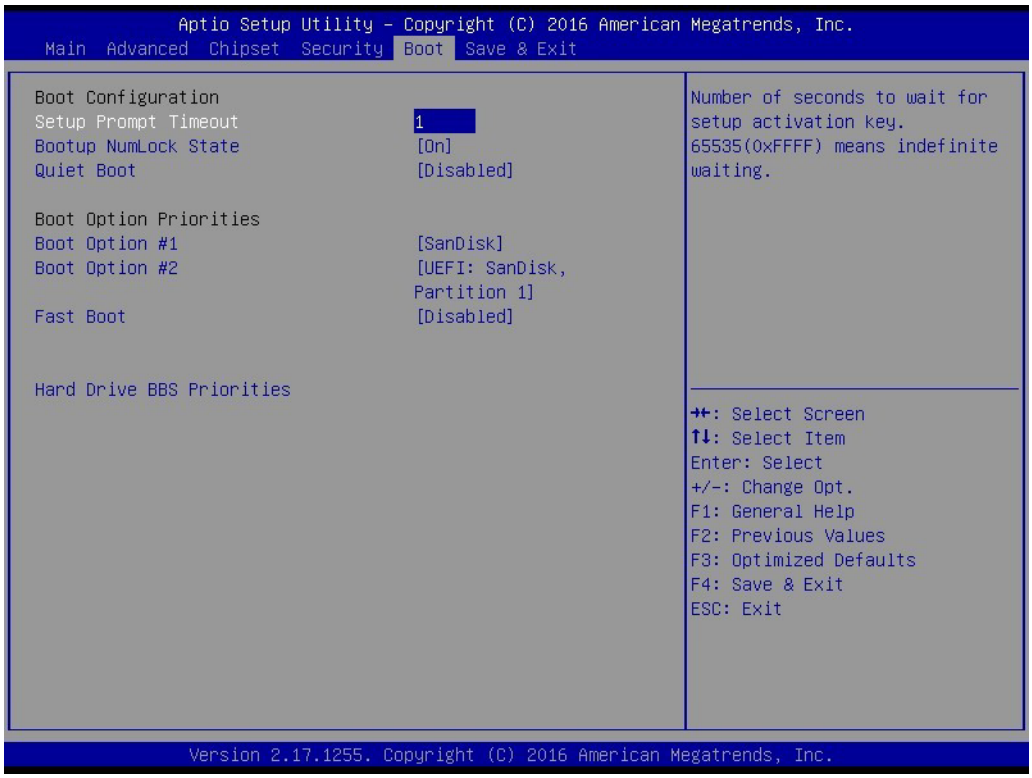
4.3.3 Security configuration



Select Security Setup from the ITA-5831 Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection are described in this section. To access the sub menu for the following items, select the item and press <Enter>. The password length is between 3 and 20.

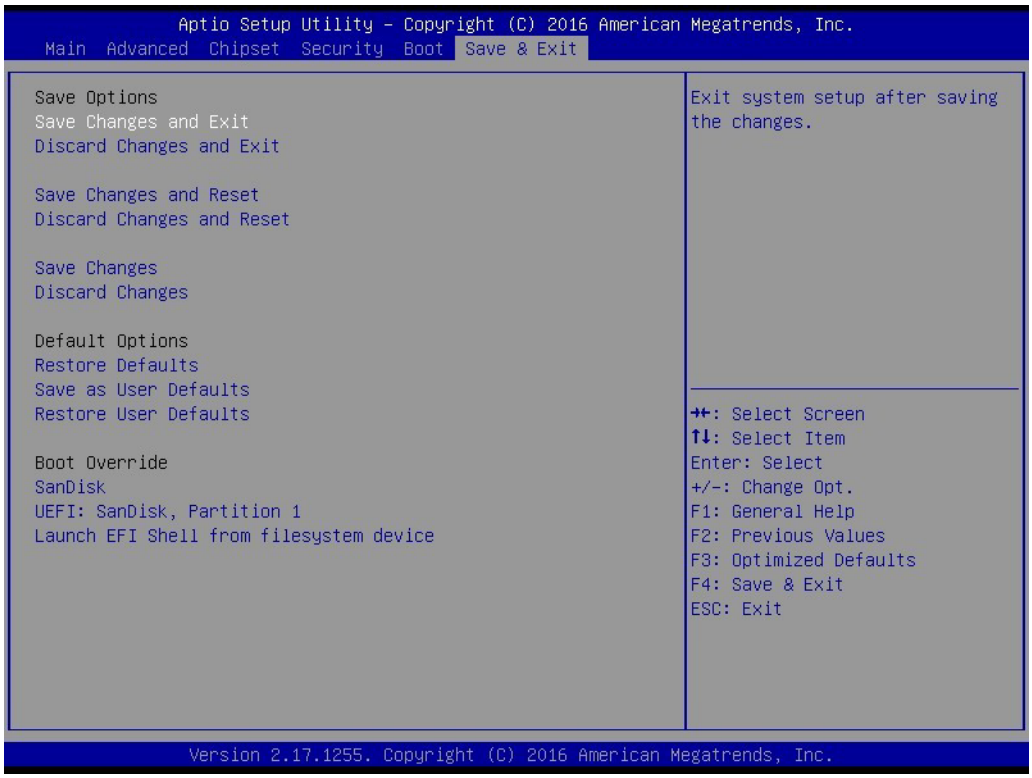
- **Administrator Password**
  Set administrator password
- **User Password**
  Set user password.

4.3.4 Boot Configuration



- **Setup Prompt Timeout**
  Set the number of seconds to wait for setup activation key. The default setting is [1].
- **Bootup NumLock State**
  Select the [NumLock] key in keyboard state. The default setting is [ON].
- **Quiet Boot**
  Enable/disable quiet boot. The default setting is [Disabled].
- **Boot Option Priorities**
  Show the system boot order.
- **Fast Boot**
  Enable/disable boot with initialization of a minimal set of devices required to launch active boot option.
- **Hard Drive BBS Priorities**
  Set the order of the legacy devices in this group.

4.3.5 Save & Exit Configuration



- **Save Changes and Exit**
  Exit system setup after saving the changes.
- **Discard Changes and Exit**
  Exit system setup without saving any changes.
- **Save Changes and Reset**
  Reset the system after saving the changes.
- **Discard Changes and Reset**
  Reset the system setup without saving any changes.
- **Save Changes**
  Save changes done so far to any of the setup options.
- **Discard Changes**
  Discard changes done so far to any of the setup options.
- **Restore Defaults**
  Restore/Load default values for all the setup settings.
- **Save as User Defaults**
  Save the changes done so far as user defaults.
- **Restore as User Defaults**
  Restore the user defaults to all the setup options.

Chapter 5

Driver Installation

Sections include:

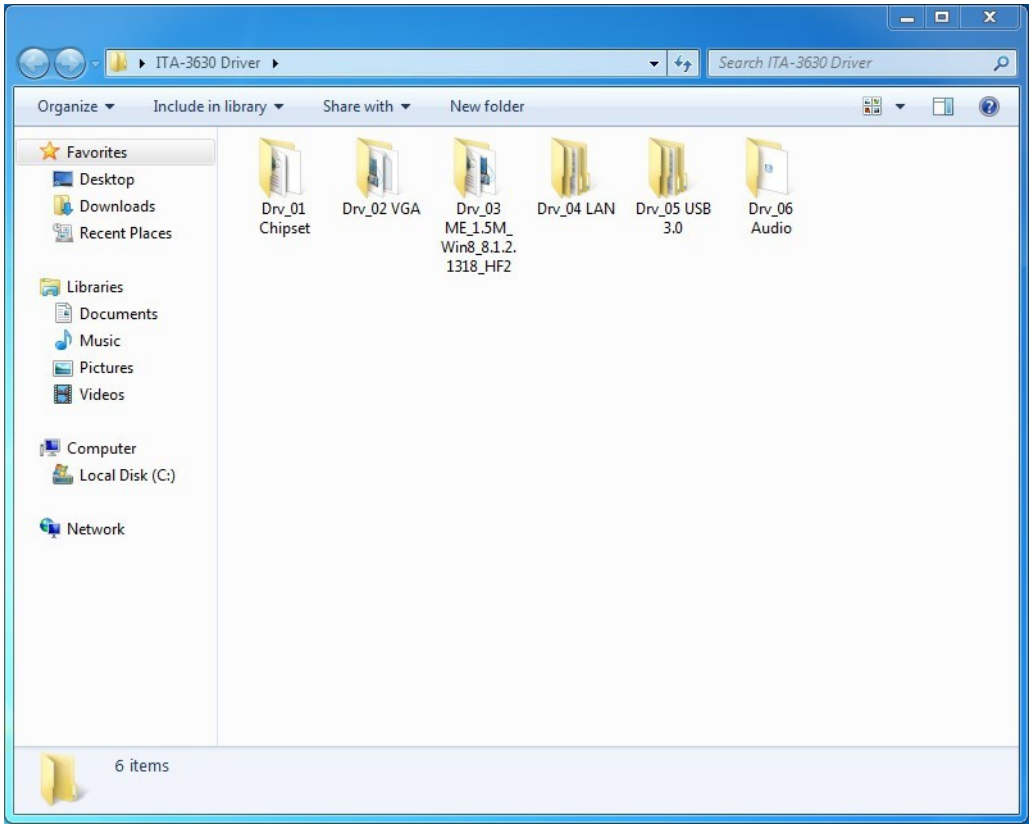
- Chipset Windows Driver Setup
- VGAWindows Driver Setup
- ME Windows Driver Setup
- LAN Windows Driver Setup
- USB 3.0 Windows Driver Setup

5.1 Introduction

Advantech offers a complete range of device driver and software supports for Windows programming developers. You can apply the Windows Device Drivers to the most popular Windows Programming tools, such as Visual C++, Visual Basic, Borland C++ Builder and Borland Delphi. Here Windows 7 is taken as an example.

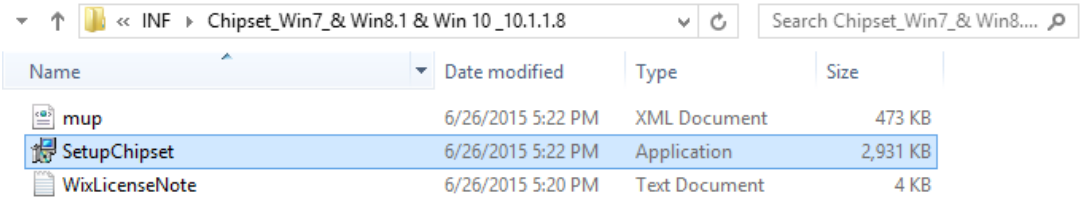
5.2 Driver Installation

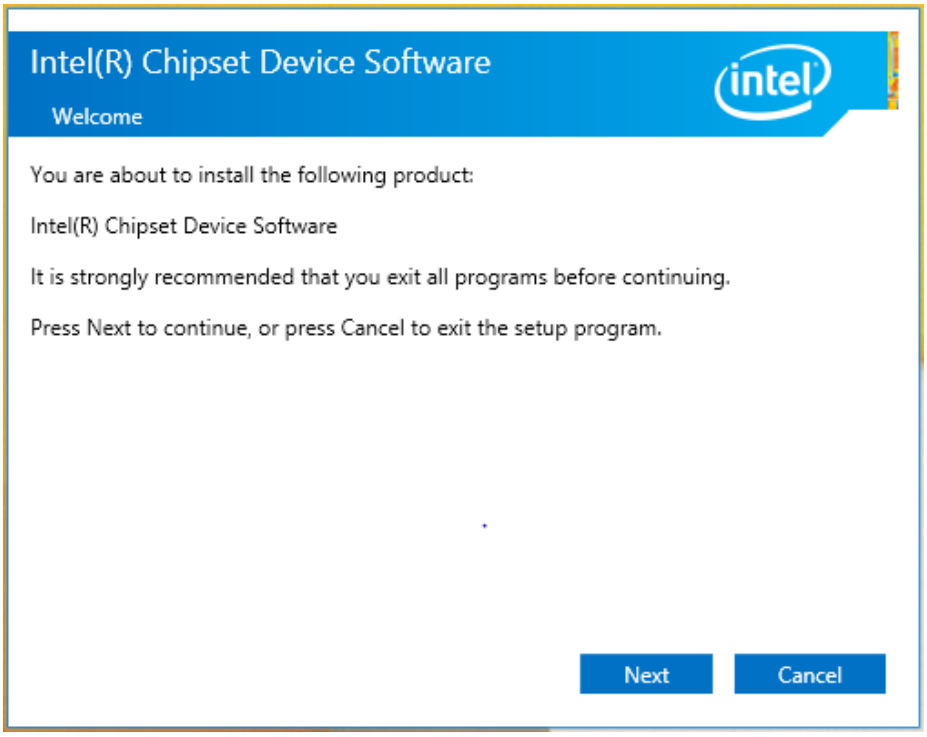
Insert the driver CD into your system's CD-ROM driver. You can see the ITA-5831 driver folder items.

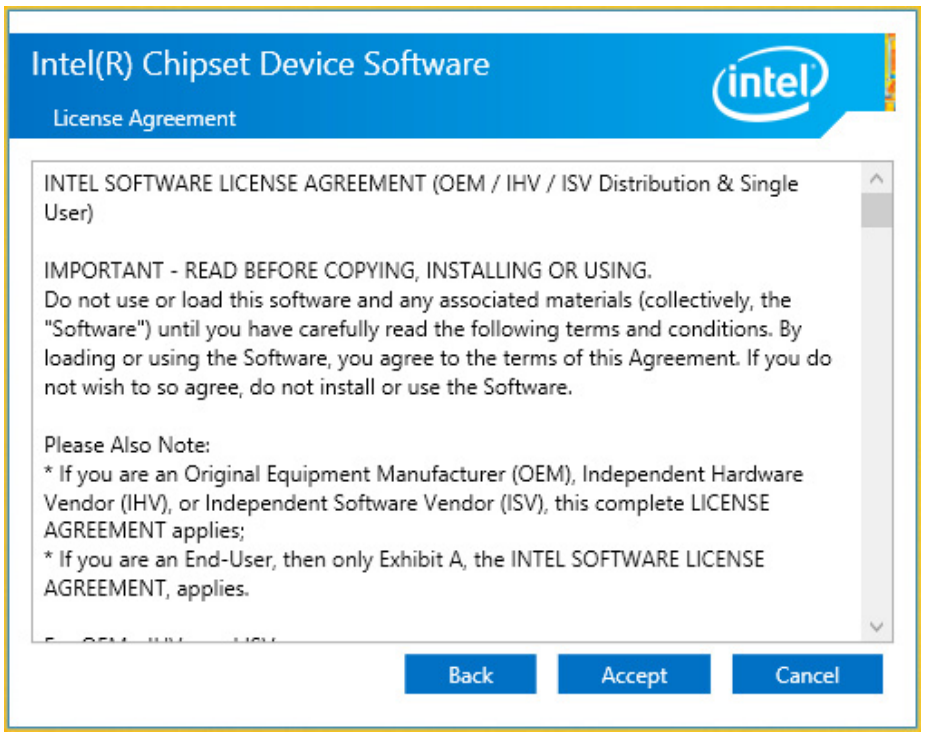


5.2.1 Chipset Windows Driver Setup

Insert the driver CD into your system's CD-ROM driver. You can see the driver folder items. Navigate to the "INF" folder and click "Setup" to complete the installation.



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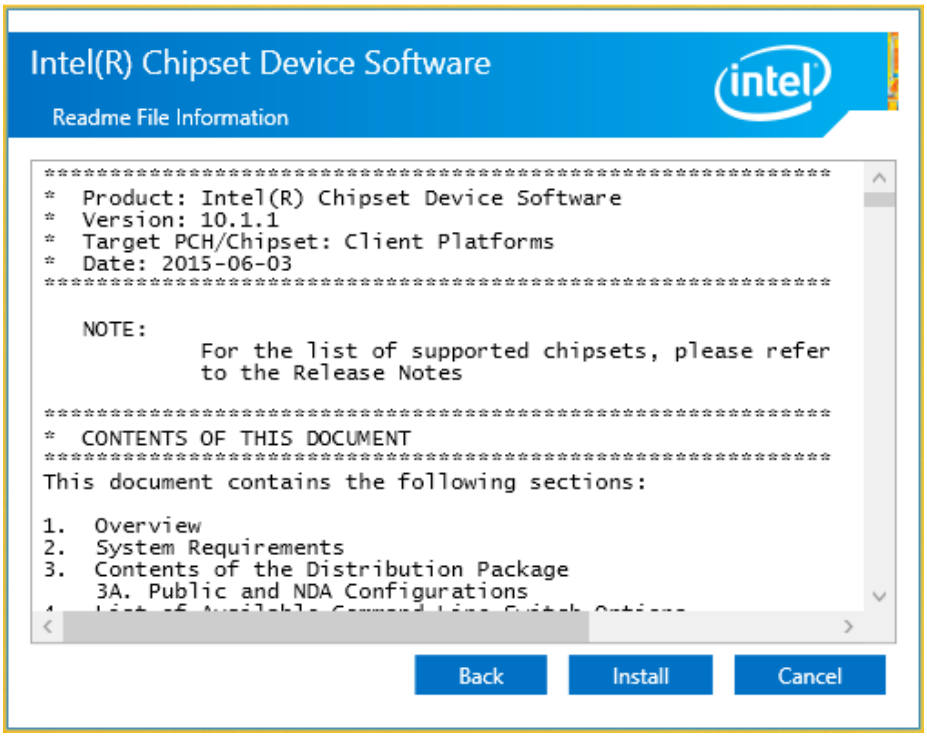
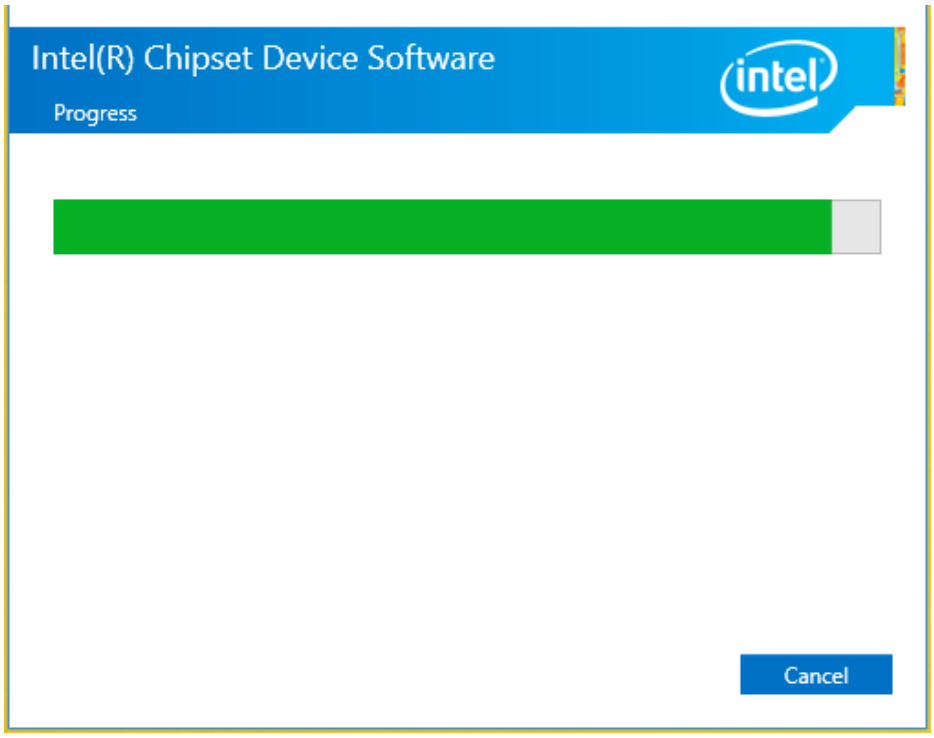
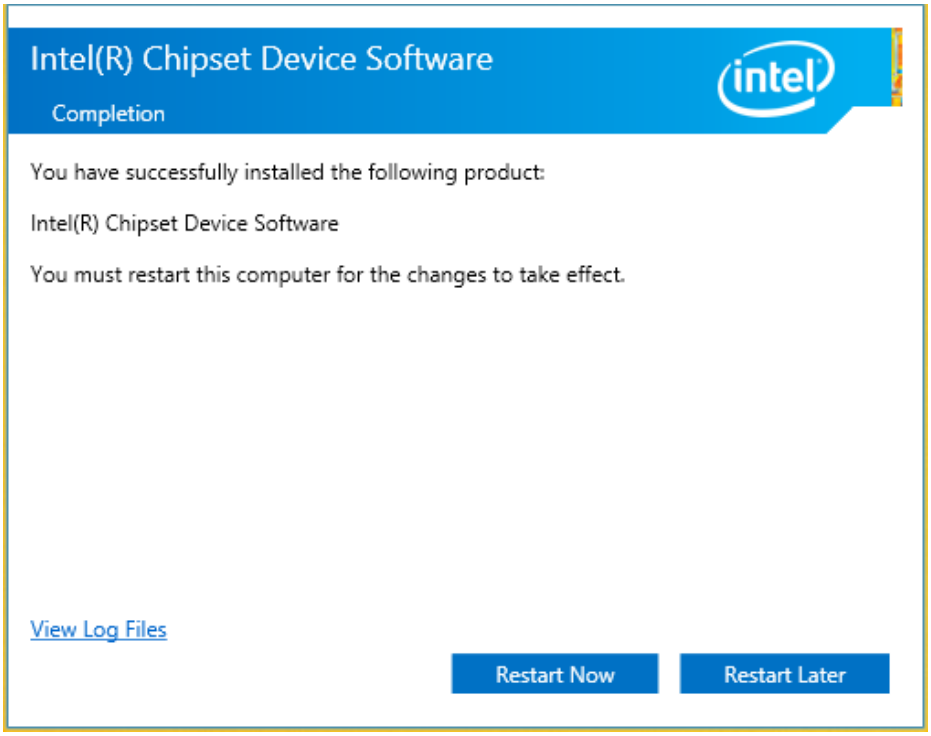
Back
Accept
Cancel

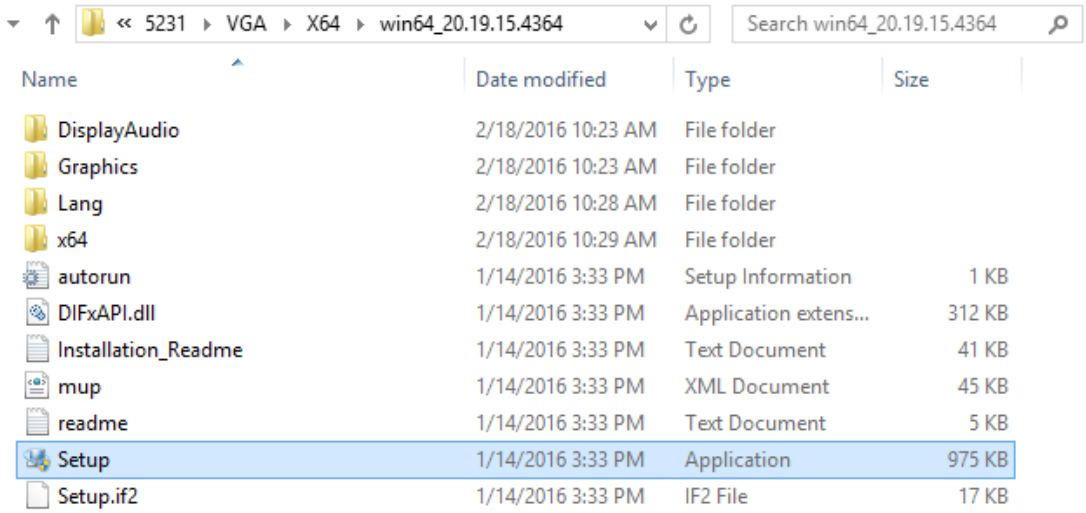

Intel(R) Chipset Device Software
Readme File Information
* Product: Intel(R) Chipset Device Software
* Version: 10.1.1
* Target PCH/Chipset: Client Platforms
* Date: 2015-06-03
NOTE:
For the list of supported chipsets, please refer to the Release Notes
* CONTENTS OF THIS DOCUMENT
This document contains the following sections:
1. Overview
2. System Requirements
3. Contents of the Distribution Package
3A. Public and NDA Configurations
Back
Install
Cancel


Intel(R) Chipset Device Software
Progress
Cancel


Intel(R) Chipset Device Software
Completion
You have successfully installed the following product:
Intel(R) Chipset Device Software
You must restart this computer for the changes to take effect.
View Log Files
Restart Now
Restart Later

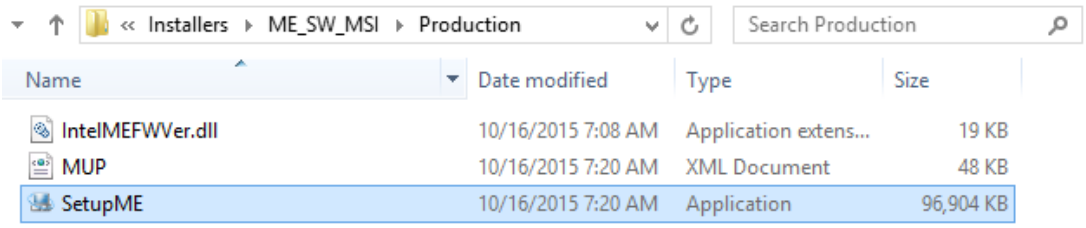
5.2.2 VGA Windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the driver folders items. Navigate to the "VGA" folder and click "Setup" to complete the installation of the drivers.



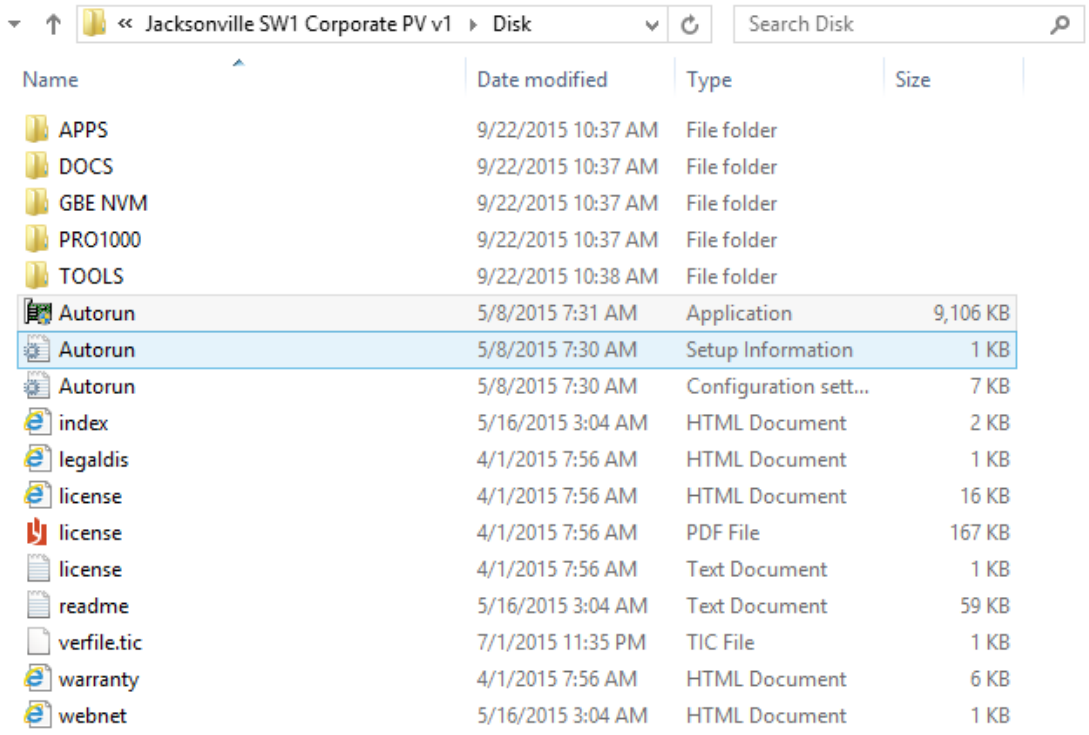
5.2.3 ME Windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the driver folders items. Navigate to the "ME" folder and click "Setup" to complete the installation of the drivers.



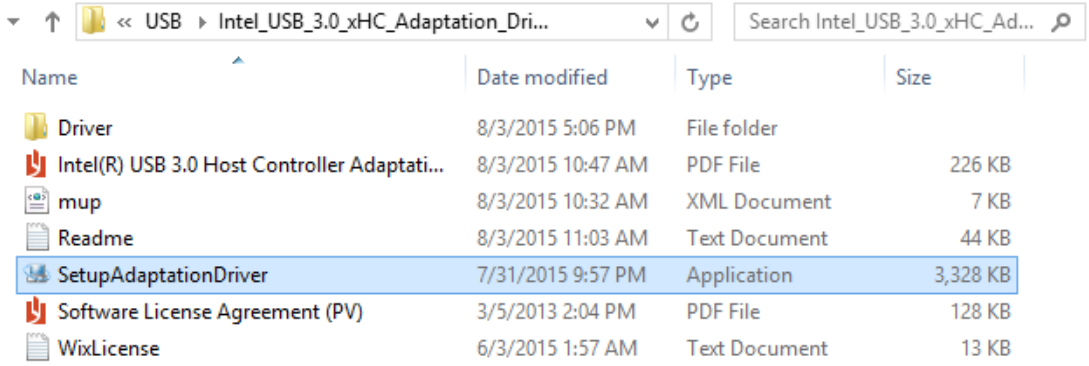
5.2.4 LAN Windows Driver Setup

Insert the driver CD into your system's CD-ROM drive. You can see the driver folders items. Navigate to the "LAN" folder and click "Setup" to complete the installation of the drivers.



5.2.5 US3.0 Windows Driver Setup

Insert the driver CD into your system's CD-ROM driver. You can see the driver folders items. Navigate to the "USB" folder and click "Setup" to complete the installation of the drivers.



5.2.6 Audio Windows Driver Setup

Insert the driver CD into your system's CD-ROM driver. You can see the driver folders items. Navigate to the "Aduio" folder and click "Setup" to complete the installation.

Chapter 6

GPIO Programming Guide

This chapter introduces GPIO programming Guide.

Note! *Please download the NXP Semiconductors PAC9554 spec for programming from NXP's website.*

https://www.nxp.com/docs/en/data-sheet/PCA9554_9554A.pdf?fsrch=1&sr=1&pageNum=1

6.1 ITA-5831 Digital DIO Definition

See Section 2.3.3.

6.2 Configuration Sequence

ITA-5831's GPIO is realized through PCA9554 GPIO IC connected to ICH SMBUS. Therefore, the configuration and access to GPIO IC is completed by IO Space accessing to ICH SMBUS controller.

Table 6.1: ICH SMBUS IO Space

SMB_BASE+ Offset	Mnemonic	Register Name	Default	Type
00h	HST_STS	Host Status	00h	R/WC,RO, R/WC (special)
02h	HST_CNT	Host Control	00h	R/W,W O
03h	HST_CMD	Host Command	00h	R/W
04h	XMIT_SLVA	Transmit slave address	00h	R/W
05h	HST_D0	Host Data 0	00h	R/W
06h	HST_D1	Host Data 1	00h	R/W

For ITA-5831, IO address of the above SMB_BASE is 0xF040. The detailed SMBUS IO control access code, please refer to Chapter 3.The corresponding SMBUS slave address of PCA9554 of GPIO 00 - GPIO 07 on ITA-5831 is 0x40 (8bit address):

GPIO 00 – GPIO 07: PCA9554 0x40 (IO0 – IO7)

Table 6.2: Pin Define

Symbol	PinDIP16, SO16, SSOP16, TSSOP16	HVQFN16	SSOP20	Description
A0	1	15	6	Address input 0
A1	2	16	7	Address input 1
A2	3	1	9	Address input 2
IO0	4	2	10	Input/output 0
IO1	5	3	11	Input/output 1
IO2	6	4	12	Input/output 2
IO3	7	5	14	Input/output 3
VSS	8	6	15	Supply ground
IO4	9	7	16	Input/output 4
IO5	10	8	17	Input/output 5
IO6	11	9	19	Input/output 6
IO7	12	10	20	Input/output 7
INT	13	11	1	Interrupt output (open-drain)
SCL	14	12	2	Serial clock line
SDA	15	13	4	Serial data line
VDD	16	14	5	Supply voltage

Table 6.2: Pin Define				
n.c.	-	-	3,8,13,18	Not connected

6.2.1 Command byte

Table 6.3: Command Byte		
Command	**Protocol**	**Function**
0	Read byte	Input Port register
1	Read/Write byte	Output Port register
2	Read/Write byte	Polarity inversion register
3	Read/Write byte	Configuration register

The command byte is the first byte to follow the address bute during a write transmission. It is used as a pointer to determine which of the following registers will be written or read. PCA9554 has in all 4 registers to control GPIO.

6.2.2 PCA9554 Register 0

The register is a read-only port. It reflects in incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writer to the register Have no effect.

The default 'X' is determined by the externally applied logic level, normal '1' when no external signal applied because of the internal pull-up resistors.

Table 6.4: Register 0 – Input Port register bit description				
Bit	**Symbol**	**Access**	**Value**	**Description**
7	I7	Read only	X	Determined by externally applying logic level
6	I6	Read only	X	
5	I5	Read only	X	
4	I4	Read only	X	
3	I3	Read only	X	
2	I2	Read only	X	
1	I1	Read only	X	
0	I0	Read only	X	

If one GPIO Pin is set to Input, you can read input value from the bit that register 0 corresponds to.

6.2.3 PCA9554 Register 1 – Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Registers 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the fili-flop controlling the output selection, not the actual pin value.

Table 6.5: Register 1 – Output Port register bit description

Bit	Symbol	Access	Value	Description
7	O7	R	1*	Determined by externally applying logic level
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

If one GPIO Pin is set to Output, you can read input value from the bit that register 1 corresponds to.

6.2.4 PCA9554 Register 2 – Polarity Inversion register

The register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (write with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (write with '0'), the Input Port data polarity is retained.

Table 6.6: Register 2 – Polarity Inversion register bit description

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	Invert polarity of Input Port register data
6	N6	R/W	0*	
5	N5	R/W	0*	0= Input Port register data retained (Default value)
4	N4	R/W	0*	
3	N3	R/W	0*	1= Input Port register data inverted
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

If one GPIO Pin is set to Input, you can control the polarity of input pin from the bit that register 2 corresponds to.

6.2.5 PCA9554 Register 3 – Configuration register

The register configures the directions of the I/O pins. If a bit this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with weak pull-up to VDD.

Table 6.7: Register 2 – Polarity Inversion register bit description

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	Configures the directions of the I/O pins
6	C6	R/W	1*	
5	C5	R/W	1*	0= corresponding port pin is enabled as an
4	C4	R/W	1*	OUTPUT
3	C3	R/W	1*	1= In corresponding port pin is enabled as an INPUT (Default value)
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

Register 3 is used to set each GPIO as Input or Output:

If the bit is ‘0’, the corresponding GPIO pin is set as Output;

If the bit is ‘1’, the corresponding GPIO pin is set as Input.

6.3 Example

Here take ITA-5831 as an example. Assume GPIO 00 is set as Output and GPIO 7 is set as Input, with two pins interconnected, how to set the corresponding register?

GPIO 00 corresponds to PCA9554 0x40 IO0, while GPIO 07 corresponds to PCA9554 0x40 IO7.

Set GPIO 00 as Output:

1. Read SMBUS slave 0x40 register 3 byte value;
2. Set bit 0 of the value read in step 1 as 0 and write it to SMBUS slave 0x40 Register 3;
3. Read SMBUS slave 0x40 register 1 byte value;
4. Set bit 0 of the value read in step 3 as 0 or 1 according to low or high of the output value, then write it back to SMBUS slave 0x40 register 1.

Set GPIO 07 as Input:

1. Read SMBUS slave 0x40 register 3 byte value;
2. Set bit 7 of the value read in step 1 as 1 and write it to SMBUS slave 0x40 Register 3;
3. Read SMBUS slave 0x40 register 0 byte value;
4. Decide low or high of the input value through bit7 value read in step3.

Function call for reference:

```
ICH SMBUS Access Code
(The following code is realized by simulating the access of BIOS to
SMBUS. It uses Borand C++.
3.1 for compiling and is successfully tested under DOS (But it is not
tested under other OSs).

#define SMBUS_PORT 0xF040 //SMB_BASE is 0xF040
typedefunsigned char BYTE;

////////////////////////////////////////////////////////////////////

BYTE   smbus_read_byte(BYTE addr, BYTE offset)
//Read SMBUS Register byte value. Read one byte value each time. ddr
is slave
address (such as 0x40), and offset is register offset.
{
       int  i;
       BYTE data;

       outportb(SMBUS_PORT + 4, (addr | 1)); //Write slave address to
SMB_BASE + 4 (When reading, bit 0 of slave address should be set as 1,
so here addr|1 is available)
       newiodelay();      //delay
       newiodelay();      //delay

       chk_smbus_ready(); //Whether SMBUS is ready

       outportb(SMBUS_PORT + 3, offset);//Write register offset to
SMB_BASE  +3.
       newiodelay();      //delay
       newiodelay();      //delay

       outportb(SMBUS_PORT + 2, 0x48); //Write   SMBUS   command   to
SMB_BASE + 2. 0x48 means starting byte data transmission
       newiodelay();      //delay
       newiodelay();      //delay

       for (i = 0; i <= 0x100;  i++)
       {
            newiodelay();      //longerdelay
       }
```

```
        chk_smbus_ready(); //wheater SMBUS is ready return
(inportb(SMBUS_PORT + 5)); // Byte value read from SMB_BASE + 5
}

////////////////////////////////////////////////////////////////////

void smbus_write_byte(BYTE addr, BYTE offset, BYTE value)
// Write SMBUS Register byte value. Write one byte value each time.
addr is slave address (such as 0x40), and offset is register offset
{
        int  i;

        outportb(SMBUS_PORT + 4, addr); //  Write  slave  address  to
SMB_BASE + 4 (When writing, slave address bit 0 should be set as 0)
        moredelay();        //longerdelay
        moredelay();        //longerdelay

        chk_smbus_ready(); //wheater SMBUS is ready

        outportb(SMBUS_PORT + 3, offset);// write register offset to
SMB_BASE  +3.
        moredelay();        //longerdelay
        moredelay();        //longerdelay

        outportb(SMBUS_PORT + 5, value);//   Write   data   value   to
SMB_BASE + 5
        moredelay();        //longerdelay
        moredelay();        //longerdelay

        outportb(SMBUS_PORT + 2, 0x48); //  Write  SMBUS  command  to
SMB_BASE + 2.. 0x48 means starting byte data transmission.
        moredelay();        //longerdelay
        moredelay();        //longerdelay

        for (i = 0; i <= 0x100; i++)
        {
             newiodelay();//longerdelay
        }
        chk_smbus_ready(); //wheater SMBUS is ready
}
```

```
//////////////////////////////////////////////////////////////////////

int    chk_smbus_ready()
// To decide whether SMBUS is ready or has completed the action, you
should wait for a long time to check whether SMBUS has successfully
transmitted the command.
Since error may rarely occurs, BIOS code does not make judgement on
the return value of this function in read and write of SUMBUS byte.
{
       int  i, result = 1;
       BYTE data;

       for (i = 0; i <= 0x800; i++)
       {
            //SMB_BASE + 0 is the value of SMBUS status
            data = inportb(SMBUS_PORT);//Read SMBUS status value once
            data = check_data(SMBUS_PORT);//Read  SMBUS  status  value
several time
            outportb(SMBUS_PORT, data); //  Write  back  SMBUS  status
value which will clear status value (Write 1 to the corresponding bit
means clearing status
            if (data & 0x02)
            {    // If bit 1 is set (which means the command is
completed), SMBUS is ready
                 result = 0;//SMBUS ready
                 break;
            }

            if (!(data & 0xBF))
            {    // If all bits are 0 except bit 2 (which means error
occurs on SMBUS), SMBUS is ready
            result = 0;        //SMBUS ready
            break;
            }

            if (data & 0x04)
            {    //  If  bit  2  is  set  (which  means  error  occurs  on
SMBUS), error occurs on SMBUS which is rarely the case
            result = 1;        //SMBUS error
            break;
            }
       }

       return result;
}
```

```
//////////////////////////////////////////////////////////////////////

BYTE   check_data (W ORD addr)
{
       int  i;
       BYTE data;

       for(i = 0; i <= 6; i++)
       {
            data = inportb(addr);
            if (data!= 0)
                 break;
       }
       return data;
}

//////////////////////////////////////////////////////////////////////

void newiodelay()
//Shorter delay
{
       outportb(0xeb, 0); // IO port 0xeb No real device occupies.
Write a value to this port can realize delay function. You can also
choose other method according to the real situation.
}

//////////////////////////////////////////////////////////////////////

void  moredelay()
//longerdelay
{
       int  i;
       for (i = 0; i < 20; i++)
       {
            outportb(0xeb, 0); // IO port 0xeb No real device occu-
pies. Write a value to this port can realize delay function. You can
also choose other method according to the real situation.
       }
}
```

```
**********************************************************************
GPIO Simcodes
(take GPIO 00 and GPIO 07 as an example)

Output High to GPIO 00:
        data = smbus_read_byte(0x40, 0x03); //Read slave 0x40 register 3 byte
        data &= 0xfe;//Set bit 0 as 0
        smbus_write_byte(0x40, 0x03, data)//write, set GPIO 00 as Output
        data = smbus_read_byte(0x40, 0x01) //Read slave 0x40 register 1
        data |= 0x01; //Set bit 0 as 1, High
        smbus_write_byte(0x40, 0x01, data) //Write, Output High value


Read Input Value from GPIO 07:
        data = smbus_read_byte(0x40, 0x03); //Read slave 0x40 register 3 byte
        data |= 0x80; //Set bit 7 as 1
        smbus_write_byte(0x40, 0x03,data) //Write, set GPIO 07 as Input
        data = smbus_read_byte(0x40, 0x00) //Read slave 0x40 register
0. Then, the response value of bit 7 should know whether the input is
low or high
```

Appendix A

A Programming the Watchdog Timer

A.1 Programming the Watchdog Timer

The ITA-5831's watchdog timer can be used to monitor system software operation and take corrective action if the software fails to function within the programmed period. This section describes the operation of the watchdog timer and how to program it.

A.1.1 Watchdog Timer Overview

The watchdog timer is built into the embedded controller. It provides the following user-programmable functions: Can be enabled or disabled via user program Time-base is 100ms. Each time limit is word long. You can setup event time from 0 to 0xFFFE. Write 0xFFFF to time limit ram will make event disable. Timer can be set from 100ms to 109.22 minutes. Generates and resets the signal if the software fails to reset the timer before time-out.

A.1.2 Programming the Watchdog Timer

Watchdog timer logic can be accessed through EC PM2(Power Manager Channel2).PM2 is a LPC IO port channel. PM2 channel includes one command/status port and one data port. System can use command port to send command to EC or get current port status. System can send command parameter or get EC return data through data port. Normally, 0x29A is command/status port and 0x299 is data port.

Command/Status port: Port 0x29A

Action	Description
Write	Send command to EC
Read	Get EC 299/29A port status

Status which was read from 0x29A is described below:

Status from command/status port

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
X	X	X	X	X	X	IBF (Input buffer full)	OBF (Output buffer full)

Note!

1. *BIT0(OBF)-When EC return data to 0x299 port, OBF will be set 1. OBF will be clear to zero after system read data from 0x299 port.*
2. *BIT1(IBF)-When system write data or command to 0x299 or 0x29A, IBF will be set 1. IBF will be clear to zero after EC get data/ command from 299/29A port.*

Data Port: Port 0x299

Action	Description Send
Write	data to EC Get
Read	data from EC

Note!

1. *After you write data/command to 299/29A port, IBF will be set 1. You must wait IBF clear to zero, then you can write next data/command to 299/29A port.*
2. *If EC command will return data, you read data from 68 port when OBF is set to 1.*

Watchdog Command

0x28	Start watchdog
0x29	Stop watchdog
0x2A	Reset watchdog
0x88	Read EC HW ram
0x89	Write EC HW ram

Watchdog HW Ram address

Watchdog HW Ram is used to setup time limit and also keep event status.

Address	Function	Description							
0x57	Watch dog event flag	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		X	X	X	PwrBtn	WDPIN	RESET	SCI	NMI
0x5E-0x5F	Watchdog reset delay time	0~0xFFFE, setup reset time							

Note!

NMI – 1: NMI event sent. 0:not sent SCI
– 1: SCI event sent. 0:not sent
RESET – 1: RESET event sent. 0:not sent
WDPIN – 1: Watchdog output pin event sent. 0:not sent
PwrBtn – 1: Power button event sent. 0:not sent

Example Program

```
//Wait IBF Empty
unsigned char ECWaitIBFEmpty()
{
	unsigned char Status;

	do{
	     Status = inportb(0x29A);    //Read back Status
	} while (Status & 0x02); //If IBF Set?

	return Status;
}

//Write non-data command (no data) to EC
void EcWriteCmd (unsigned char cmd)
{
	ECWaitIBFEmpty();//Wait IBF Empty outpor tb(0x29A, (unsigned
char)cmd);   //Write command
}

//Write standard command (include data) to EC
void IT8528ECSetData (
	unsigned char	Cmd, //command
	unsigned char	Addr,//write address
	unsigned char	Value,//data
)
{
	ECWaitIBFEmpty();                          //Wait IBF Empty
	outportb (IT8528E_HWM_CMD_PORT, Cmd);      //Write command
	ECWaitIBFEmpty();                          //Wait IBF Empty
	outportb (IT8528E_HWM_DATA_PORT, Addr); //Write address
	ECWaitIBFEmpty();                          //Wait IBF Empty
	outportb (IT8528E_HWM_DATA_PORT, Value);   //Write data
}

//Stop watchdog
void disable_wdt()
{
	EcWriteCmd(0x29);       //Write command 0x29 to stop watch dog
}
```

```
//Start watchdog
void enable_wdt( i
       nt time,       //Time
       int timebase   //Time base: 0: second 1: minute
)
{
       unsigned int time_word;

       EcWriteCmd(0x29);  //Write command 0x29 to stop watch dog

       if (timebase == 0) //Second base = 100ms * 10
            time_word = time * 10;
       else               //Minute base = 100ms * 600
            time_word = time * 600;

       IT8528ECSetData (0x89,0x5E, (unsigned char)(time_word>>8));//Use
command 0x89 to write time data hibyte to hw ram address 0x5E
       IT8528ECSetData (0x89, 0x5F,(unsigned char)(time_word&0x00ff)); //Use
command 0x89 to write time data lowbyte to hw ram address 0x5f
       IT8528ECSetData (0x89, 0x57, 0x04);                    //Use
command 0x89 to write watchdog time event to hw ram address
0x57
                                                              //0x04:
Bit2 =1 , watchdog output as RESET

       EcWriteCmd(0x28);///Write command 0x28 to stop watch dog
}
```

Appendix B

Declaration of A the Presence Condition of the Restricted Substances Marking

BSMI RoHS 限用物質含有情況標示確認表

Declaration of the Presence Condition of the Restricted Substances Marking

設備名稱：電腦 Equipment name	型號 （型式）：ITA-5831 Type designation (Type)					
單元 Unit	限用物質及其化學符號 Restricted substances and its chemical symbols					
	鉛 Lead (Pb)	汞 Mercury (Hg)	鎘 Cadmium (Cd)	六價鉻 Hexavalent chromium (Cr^{+6})	多溴聯苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)
電路板	－	○	○	○	○	○
固定组件 （螺絲、螺柱）	－	○	○	○	○	○
內外殼	○	○	○	○	○	○
散熱模組	○	○	○	○	○	○
線材	－	○	○	○	○	○

備考 1.“ 超出 0.1 wt %” 及 “ 超出 0.01 wt %” 係指限用物質之百分比含量超出百分比含量基準值。

Note 1: “Exceeding 0.1 wt %” and “exceeding 0.01 wt %” indicate that the percentage content of the restricted substance exceeds the reference percentage value of presence condition.

備考 2.“ ○ ” 係指該項限用物質之百分比含量未超出百分比含量基準值。

Note 2: “○” indicates that the percentage content of the restricted substance does not exceed the percentage of reference value of presence.

備考 3.“ － ” 係指該項限用物質為排除項目。

Note 3” The “-” indicates that the restricted substance corresponds to the exemption.

Appendix C

Safety Instructions
Battery Information

C.1 安全指示

1. 請仔細閱讀此安全操作說明。
2. 請妥善保存此用戶手冊供日後參考。
3. 用濕抹布清洗設備前，請從插座拔下電源線。請不要使用液體或去汙噴霧劑清洗設備。
4. 對於使用電源線的設備，設備周圍必須有容易接觸到的電源插座。
5. 請不要在潮濕環境中使用設備。
6. 請在安裝前確保設備放置在可靠的平面上，意外跌落可能會導致設備損壞。
7. 設備外殼的開口是用於空氣對流，從而防止設備過熱。**請不要覆蓋這些開口。**
8. 當您連接設備到電源插座上前，請確認電源插座的電壓是否符合要求。
9. 請將電源線佈置在人們不易絆到的位置，並不要在電源線上覆蓋任何雜物。
10. 請注意設備上的所有警告標識。
11. 如果長時間不使用設備，請將其同電源插座斷開，避免設備被超標的電壓波動損壞。
12. 請不要讓任何液體流入通風口，以免引起火災或者短路。
13. 請不要自行打開設備。為了確保您的安全，請由經過認證的工程師來打開設備。如遇下列情況，請由專業人員來維修：
    - 電源線或者插頭損壞；
    - 設備內部有液體流入；
    - 設備曾暴露在過於潮濕的環境中使用；
    - 設備無法正常工作，或您無法通過用戶手冊來使其正常工作；
    - 設備跌落或者損壞；
    - 設備有明顯的外觀破損。
14. 請不要把設備放置在超出我們建議的溫度範圍的環境，即不要低於 -25° C（-13° F）或高於 60° C （140° F），否則可能會損壞設備。
15. 此為 A 級產品，在生活環境中，該產品可能會造成無線電干擾。在這種情況下，可能需要使用者對干擾採取切實可行的措施。
16. 本產品不帶電線元件銷售，應購買已通過 CCC 認證的電線元件。

注意：電腦配置了由電池供電的即時時鐘電路，如果電池放置不正確，將有爆炸的危險。因此，只可以使用製造商推薦的同一種或者同等型號的電池進行替換。請按照製造商的指示處理舊電池。

根據 IEC 704-1:1982 的規定，操作員所在位置的聲壓級不可高於 70dB(A)。

免責聲明：該安全指示符合 IEC 704-1 的要求。研華公司對其內容的準確性不承擔任何法律責任。

C.2 電池信息

電池、電池組和蓄電池不應作為未分類的生活垃圾處理，請使用公共收集系統返回和回收，或哪找當地法規要求進行處理。

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